JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

B.Tech – II-I Sem

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19A04302T ELECTRONIC DEVICES AND CIRCUITS

Course Objectives:

- To acquire fundamental knowledge and expose to the field of semiconductor theory and devices and their applications.
- To introduce different types of semiconductor devices, viz., diodes and special diodes.
- To explain application of diodes as rectifiers, clippers, clampers and regulators.
- To describe operation and characteristics of Bipolar Junction Transistor& Field Effect Transistor.
- To analyze the various biasing circuits using BJTs & FETs.

Unit I:

Semiconductor Diode: Open circuited PN junction, PN junction as a rectifier, Current components in a PN diode, Diode Equation and its mathematical derivation, Volt-Ampere Characteristics, Energy band diagram of PN diode, Temperature dependence of Volt-Ampere Characteristics, Diode resistance (Static and Dynamic resistance), Transition capacitance, Diffusion capacitance, Step graded junction.

Unit II:

Special Devices: Avalanche breakdown, V-I Characteristics of Zener diode, Zener breakdown, Principle of operation and characteristics of Tunnel diode with the help of Energy band diagram, Photo diode, LED, PIN diode and Varactor diode, Silicon Controlled Rectifier (SCR) and its V-I characteristics, DIAC, TRIAC, Schottky Barrier diode, solar cell, Uni-Junction Transistor (UJT) and its V-I Characteristics, Problem solving.

Unit III:

Diode Applications: Diode as switch, Rectifier – Half wave and Full wave rectifier, Bridge rectifier, Ripple factor, PIV, Filters – Inductor and Capacitor Filter, L-section filter, pi-Filter, Zener as voltage regulator, Clipping and Clamping circuits, Detector, Voltage doubler, Problem solving related to diode applications.

Unit IV:

Bipolar Junction Transistor (BJT):
Transistor – Structure, current components and their relationship, PNP and NPN transistors- Active mode of operation, symbols and conventions, Transistor equations, Transistor as an amplifier, input and output characteristics of Common Base, Common Emitter and Common collector configurations. DC analyses of Common Base, Common Emitter and Common collector circuits.

BJT Biasing: Load line and modes of operations, operating point, Bias stability, fixed bias, self bias, stabilization against variations in I_{co}, V_{BE}, β, Bias compensation, Thermal runaway, condition for Thermal stability, Problem solving.

Applications: As a switch, as an amplifier.

Unit V:

Field-Effect Transistors (FET) : Metal Oxide Semiconductor Field-effect Transistor (MOSFET) - structures and V-I characteristics of n-channel Enhancement mode MOSFET, p-channel Enhancement mode MOSFET, n-channel depletion mode MOSFET, p-channel depletion mode MOSFET, symbols and conventions, Complementary MOSFETs (CMOSFETs) - structure, V-I characteristics, symbols and conventions, structure and V-I characteristics of n-channel and p-channel Junction Field Effect Transistors (JFET), Problem solving.

Biasing Circuits Using MOSFETS and JFETS: Different configurations using MOSFETs and JFET, load line and modes of operation, different biasing circuits (self-bias, voltage divider bias) using MOSFETs and JFETs, DC Analysis of n-channel and p-channel MOSFETs (both Enhancement and Depletion modes),DC analysis of n-channel and p-channel JFETs, Problem solving.

Applications: MOSFETs, JFET as switch and small signal amplifier, CMOS as a switch.

Course Outcomes:

After the completion of the course students will able to

CO1: Understand principle, operation, characteristics and applications of Bipolar Junction Transistor and Field Effect Transistor (L1)

CO2: Describe basic operation and characteristics of various semiconductor devices. (L2)

CO3: Analyze diode circuits for different applications such as rectifiers, clippers and clampers also analyze low frequency and high frequency models of BJT and FET. (L3)

CO4: Design various biasing circuits for BJT and FET. (L4)

CO5: Compare the performance of various semiconductor devices. (L5)

TEXT BOOKS:

1. Donald A Neamen, “Electronic Circuits – analysis and design”, 3rd Edition, McGraw Hill (India), 2019.
2. J. Milliman and C Halkias, “Integrated electronics”, 2nd Edition, Tata McGraw Hill, 1991.

REFERENCES:

1. Behzad Razavi, “Microelectronics”, 2nd edition, Wiley, 2013.
2. R.L. Boylestad and Louis Nashelsky, “Electronic Devices and Circuits,” 9th Edition, Pearson, 2006.
3. Jimmie J Cathey, “Electronic Devices and Circuits,” Schaum’s outlines series, 3rd edition, McGraw-Hill (India), 2010.

UNIT- I
PN DIODE CHARACTERISTICS

Introduction:

Electronics Engineering is a branch of engineering which deals with the flow of electrons in vacuum tubes, gas and semiconductor.

Applications of Electronics:
Home Appliances, Medical Applications, Robotics, Mobile Communication, Computer Communication etc.

Atomic Structure:

- Atom is the basic building block of all the elements. It consists of the central nucleus of positive charge around which small negatively charged particles called electrons revolve in different paths or orbits.

- An Electrostatic force of attraction between electrons and the nucleus holds up electrons in different orbits.

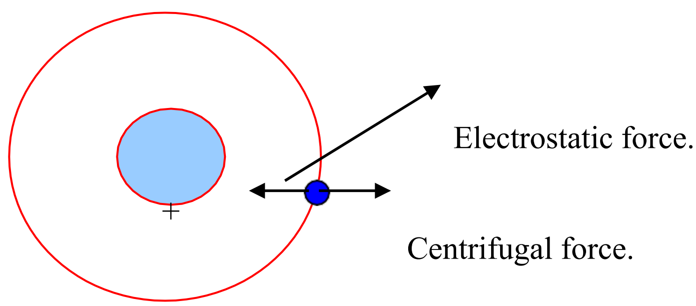


Figure 1.1: Atomic structure

- Nucleus is the central part of an atom and contains protons and neutrons. A proton is positively charged particle, while the neutron has the same mass as the proton, but has no charge. Therefore, nucleus of an atom is positively charged.

- **atomic weight = no. of protons + no. of neutrons**

- An electron is a negatively charged particle having negligible mass. The charge on an electron is equal but opposite to that on a proton. Also the number of electrons is equal to the number of protons in an atom under ordinary conditions. Therefore an atom is neutral as a whole.

- **Atomic number = no. of protons or electrons in an atom**

- The number of electrons in any orbit is given by $2n^2$ where n is the number of the orbit.

  For example, I orbit contains $2x1^2 = 2$ electrons

  II orbit contains $2x2^2 = 8$ electrons

  III orbit contains $2x3^2 = 18$ electrons and so on

- The last orbit cannot have more than 8 electrons.
- The last but one orbit cannot have more than 18 electrons.

Positive and negative ions:

- Protons and electrons are equal in number hence if an atom loses an electron it has lost negative charge therefore it becomes positively charged and is referred as positive ion.
- If an atom gains an electron it becomes negatively charged and is referred to as negative ion.

Valence electrons:

The electrons in the outermost orbit of an atom are known as valence electrons.

- The outermost orbit can have a maximum of 8 electrons.
- The valence electrons determine the physical and chemical properties of a material.
- When the number of valence electrons of an atom is less than 4, the material is usually a metal and a conductor. Examples are sodium, magnesium and aluminium, which have 1,2 and 3 valence electrons respectively.
- When the number of valence electrons of an atom is more than 4, the material is usually a non-metal and an insulator. Examples are nitrogen, sulphur and neon, which have 5,6 and 8 valence electrons respectively.
- When the number of valence electrons of an atom is 4 the material has both metal and non-metal properties and is usually a semi-conductor. Examples are carbon, silicon and germanium.

Free electrons:

- The valence electrons of different material possess different energies. The greater the energy of a valence electron, the lesser it is bound to the nucleus.
- In certain substances, particularly metals, the valence electrons possess so much energy that they are very loosely attached to the nucleus.
- The loosely attached valence electrons move at random within the material and are called free electrons.

The valence electrons, which are loosely attached to the nucleus, are known as free

electrons.

Energy bands:

- In case of a single isolated atom an electron in any orbit has definite energy.
- When atoms are brought together as in solids, an atom is influenced by the forces from other atoms. Hence an electron in any orbit can have a range of energies rather than single energy. These range of energy levels are known as Energy bands.
- Within any material there are two distinct energy bands in which electrons may exist viz , Valence band and conduction band.

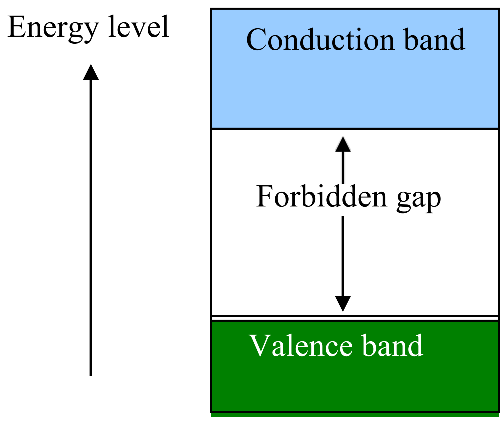


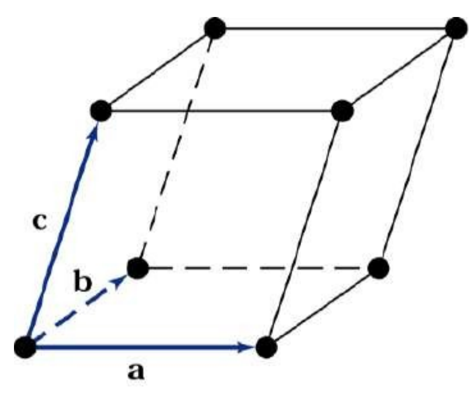
Figure 1.2: Energy level diagram

- **The range of energies possessed by valence electrons is called valence band**.
- **The range of energies possessed by free electrons is called conduction band.**
- **Valence band and conduction band are separated by an energy gap in which no electrons normally exist this gap is called forbidden gap.**

Electrons in conduction band are either escaped from their atoms (free electrons) or only weakly held to the nucleus. Thereby by the electrons in conduction band may be easily moved around within the material by applying relatively small amount of energy. (either by increasing the temperature or by focusing light on the material etc.) This is the reason why the conductivity of the material increases with increase in temperature.

But much larger amount of energy must be applied in order to extract an electron from the valence band because electrons in valence band are usually in the normal orbit around a nucleus. For any given material, the forbidden gap may be large, small or non-existent.

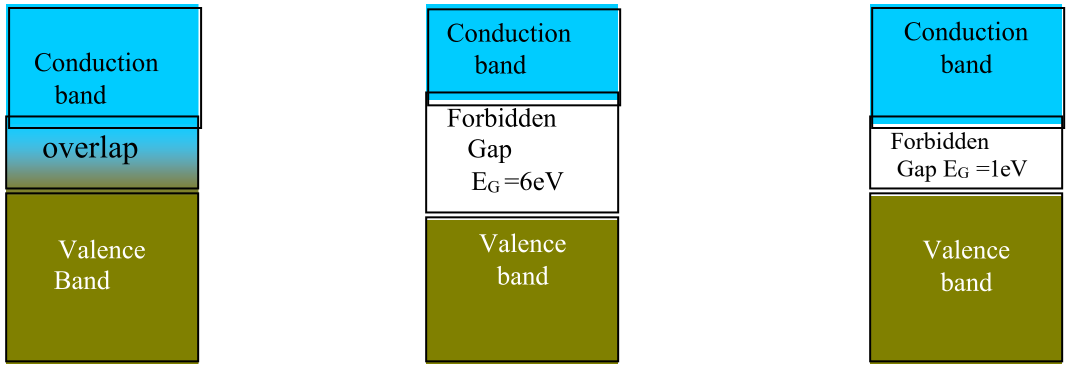
The periodic arrangement of atoms is called lattice. A unit cell of a material represents the Entire lattice. By repeating the unit cell throughout the crystal, one can generate the entire lattice.



Classification of materials based on Energy band theory:

Based on the width of the forbidden gap, materials are broadly classified as

- Conductors
- Insulators
- Semiconductors.



(a) Conductor (b) Insulator (c) Semiconductor

Conductors:

- Conductors are those substances, which allow electric current to pass through them.
  Example: Copper, Al, salt solutions, etc.

- In terms of energy bands, conductors are those substances in which there is no forbidden gap. Valence and conduction band overlap as shown in fig (a).

- For this reason, very large number of electrons are available for conduction even at extremely low temperatures. Thus, conduction is possible even by a very weak electric field.

Insulators:

- Insulators are those substances, which do not allow electric current to pass through them.
  Example: Rubber, glass, wood etc.

- In terms of energy bands, insulators are those substances in which the forbidden gap is very large.

- Thus valence and conduction band are widely separated as shown in fig (b). Therefore insulators do not conduct electricity even with the application of a large electric field or by heating or at very high temperatures.

Semiconductors:

- Semiconductors are those substances whose conductivity lies in between that of a conductor and Insulator.
  Example: Silicon, germanium, Cealenium, Gallium, arsenide etc.

- In terms of energy bands, semiconductors are those substances in which the forbidden gap is narrow.

- Thus valence and conduction bands are moderately separated as shown in fig(C).

- In semiconductors, the valence band is partially filled, the conduction band is also partially filled, and the energy gap between conduction band and valence band is narrow.

- Therefore, comparatively smaller electric field is required to push the electrons from valence band to conduction band . At low temperatures the valence band is completely filled and conduction band is completely empty. Therefore, at very low temperature a semi-conductor actually behaves as an insulator.

Conduction in solids:

- Conduction in any given material occurs when a voltage of suitable magnitude is applied to it, which causes the charge carriers within the material to move in a desired direction.

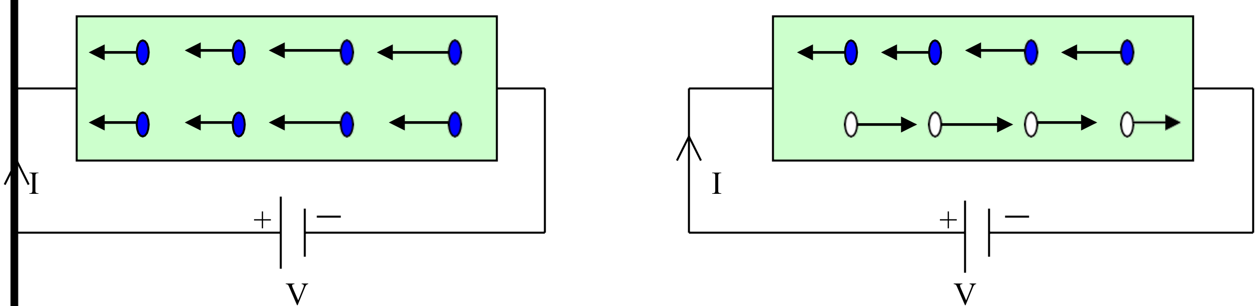
- This may be due to electron motion or hole transfer or both.

Electron motion:

Free electrons in the conduction band are moved under the influence of the applied electric field. Since electrons have negative charge they are repelled by the negative terminal of the applied voltage and attracted towards the positive terminal.

Hole transfer:

- Hole transfer involves the movement of holes.
- Holes may be thought of positive charged particles and as such they move through an electric field in a direction opposite to that of electrons.



(a) Conductor (b) Semiconductor

(a): Flow of electrons; Flow of current

(b): Flow of electrons; Flow of holes; Flow of current

- In a good conductor (metal) as shown in fig (a) the current flow is due to free electrons only.

- In a semiconductor as shown in fig (b). The current flow is due to both holes and electrons moving in opposite directions.

- The unit of electric current is Ampere (A) and since the flow of electric current is constituted by the movement of electrons in conduction band and holes in valence band, electrons and holes are referred as charge carriers.

Classification of semiconductors:

Semiconductors are classified into two types.

a) Intrinsic semiconductors.
b) Extrinsic semiconductors.

a) Intrinsic semiconductors:

- **A semiconductor in an extremely pure form is known as Intrinsic semiconductor**.
  Example: Silicon, germanium.

- Both silicon and Germanium are tetravalent (having 4 valence electrons).

- Each atom forms a covalent bond or electron pair bond with the electrons of neighboring atom. The structure is shown below.

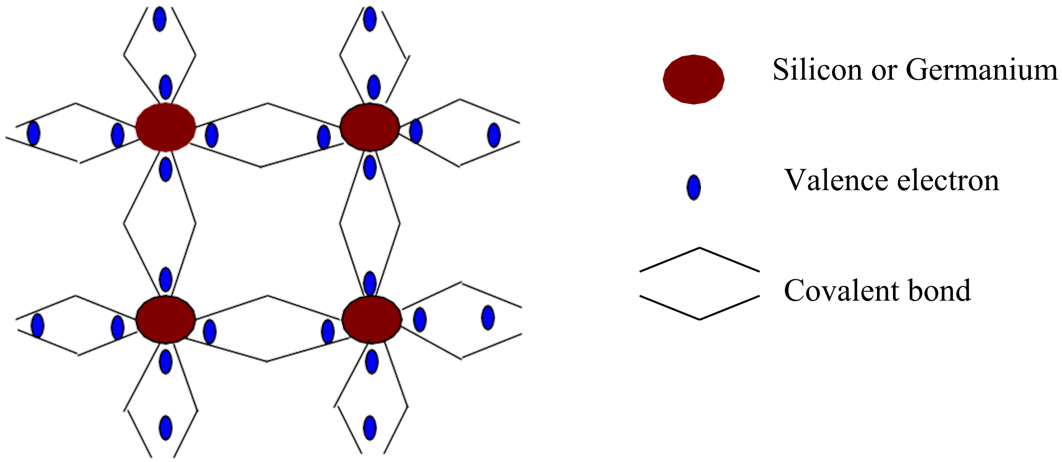


Figure 1.3: Crystalline structure of Silicon (or Germanium)

At low temperature

- At low temperature, all the valence electrons are tightly bounded the nucleus hence no free electrons are available for conduction.
- The semiconductor therefore behaves as an Insulator at absolute zero temperature.

At room temperature

- At room temperature, some of the valence electrons gain enough thermal energy to break up the covalent bonds.
- This breaking up of covalent bonds sets the electrons free and is available for conduction.
- When an electron escapes from a covalent bond and becomes free electrons a vacancy is created in a covalent bond as shown in figure above. Such a vacancy is called Hole. It carries positive charge and moves under the influence of an electric field in the direction of the electric field applied.
- Numbers of holes are equal to the number of electrons since; a hole is nothing but an absence of electrons.

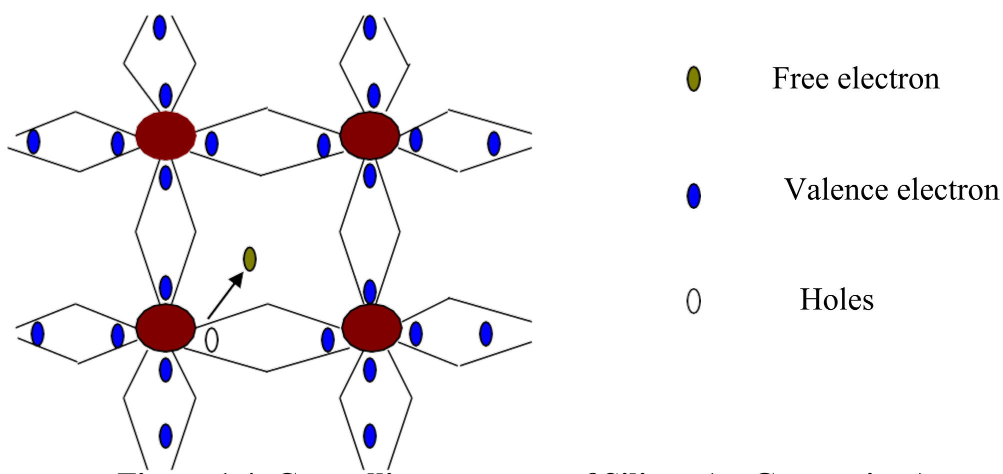


Figure 1.4: Crystalline structure of Silicon (or Germanium) at room temperature

<u>Extrinsic Semiconductor:</u>

- When an impurity is added to an intrinsic semiconductor its conductivity changes.
- This process of adding impurity to a semiconductor is called Doping and the impure semiconductor is called extrinsic semiconductor.

- Depending on the type of impurity added, extrinsic semiconductors are further classified as n-type and p-type semiconductor.

N-type semiconductor:

- **When a small current of Pentavalent impurity is added to a pure semiconductor it is called as n-type semiconductor.**
- Addition of Pentavalent impurity provides a large number of free electrons in a semiconductor crystal.
- Typical example for pentavalent impurities are Arsenic, Antimony and Phosphorus etc. Such impurities which produce n-type semiconductors are known as Donor impurities because they donate or provide free electrons to the semiconductor crystal.
- To understand the formation of n-type semiconductor, consider a pure silicon crystal with an impurity say arsenic added to it as shown in figure 1.5.
- We know that a silicon atom has 4 valence electrons and Arsenic has 5 valence electrons. When Arsenic is added as impurity to silicon, the 4 valence electrons of silicon make co-valent bond with 4 valence electrons of Arsenic.
- The 5th Valence electrons finds no place in the covalent bond thus, it becomes free and travels to the conduction band as shown in figure. Therefore, for each arsenic atom added, one free electron will be available in the silicon crystal. Though each arsenic atom provides one free electrons yet an extremely small amount of arsenic impurity provides enough atoms to supply millions of free electrons.

Due to thermal energy, still hole election pairs are generated but the number of free electrons are very large in number when compared to holes. So in an n-type semiconductor electrons are majority charge carriers and holes are minority charge carriers . Since the current conduction is pre-dominantly by free electrons(-vely charges) it is called as n-type semiconductor(n- means –ve).

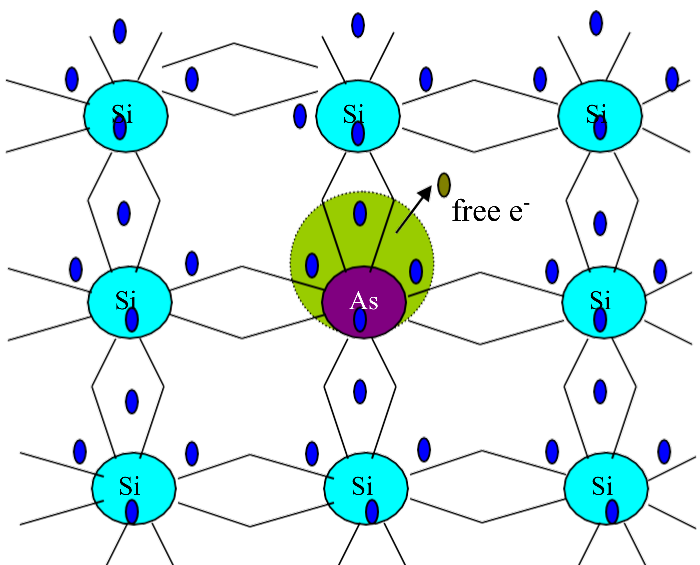


Figure 1.5: N-type semiconductors

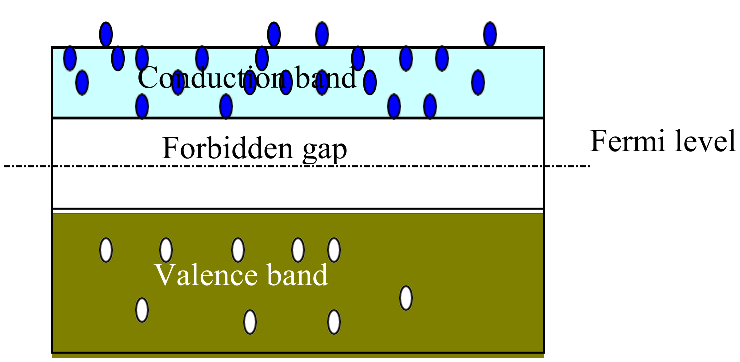


Figure 1.6: Energy band diagram for n-type semiconductor

P-type semiconductor:

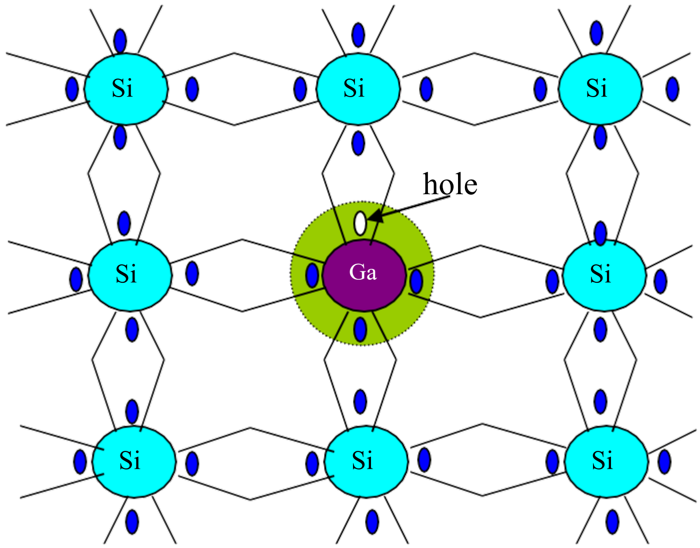


Figure 1.7: P-type semiconductor

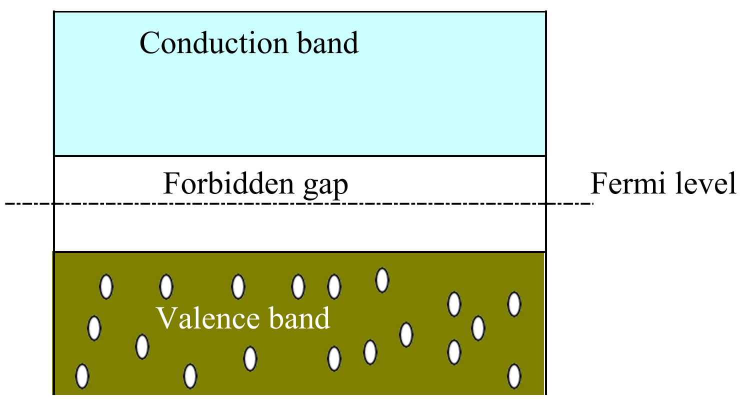


Figure 1.8: Energy band diagram for p-type semiconductor

- When a small amount of trivalent impurity is added to a pure semiconductor it is called p-type semiconductor.
- The addition of trivalent impurity provides large number of holes in the semiconductor crystals.
- Example: Gallium, Indium or Boron etc. Such impurities which produce p-type semiconductors are known as acceptor impurities because the holes created can accept the electrons in the semi conductor crystal.

To understand the formation of p-type semiconductor, consider a pure silicon crystal with an impurity say gallium added to it as shown in figure.7.

- We know that silicon atom has 4 valence electrons and Gallium has 3 electrons. When Gallium is added as impurity to silicon, the 3 valence electrons of gallium make 3 covalent bonds with 3 valence electrons of silicon.
- The 4th valence electrons of silicon cannot make a covalent bond with that of Gallium because of short of one electron as shown above. This absence of electron is called a hole. Therefore for each gallium atom added one hole is created, a small amount of Gallium provides millions of holes.

Due to thermal energy, still hole-electron pairs are generated but the number of holes is very large compared to the number of electrons. Therefore, in a p-type semiconductor holes are majority carriers and electrons are minority carriers. Since the current conduction is predominantly by hole(+ charges) it is called as p-type semiconductor (p means +ve)

PN Junction Diode:

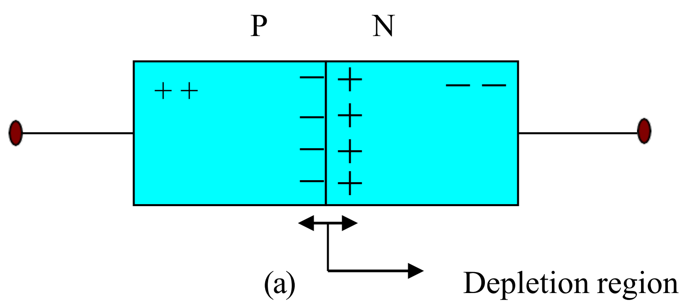
When a p-type semiconductor material is suitably joined to n-type semiconductor the contact surface is called a p-n junction. The p-n junction is also called as semiconductor diode.

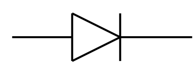
Applications of diode:

i) Used as rectifier diodes in DC power suppliers
ii) Used as clippers and clampers
iii) Used as switch in logic circuit in computers
iv) Used as voltage multipliers.

Construction and working of a PN Junction diode:

Open Circuited PN Junction:





(b)

Figure 1.9 (a): p-n junction **Figure 1.9 (b): Symbolic representation**

- The left side material is a p-type semiconductor having –ve acceptor ions and +vely charged holes. The right side material is n-type semiconductor having +ve donor ions and free electrons.

- Suppose the two pieces are suitably treated to form pn junction, then there is a tendency for the free electrons from n-type to diffuse over to the p-side and holes from p-type to the n-side . This process is called **diffusion.**

- As the free electrons move across the junction from n-type to p-type, +ve donor ions are uncovered. Hence a +ve charge is built on the n-side of the junction. At the same time, the free electrons cross the junction and uncover the –ve acceptor ions by filling in the holes. Therefore a net –ve charge is established on p-side of the junction.

- When a sufficient number of donor and acceptor ions is uncovered further diffusion is prevented.

- Thus a barrier is set up against further movement of charge carriers. This is called potential barrier or junction barrier Vo. The potential barrier is of the order of 0.1 to 0.3V.

Note: outside this barrier on each side of the junction, the material is still neutral. Only inside the barrier, there is a +ve charge on n-side and –ve charge on p-side. This region is called depletion layer.

Biasing of a PN junction diode:

Connecting a p-n junction to an external DC voltage source is called biasing.

1. Forward biasing
2. Reverse biasing

1. Forward biasing

- When external voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow is called forward biasing.

- To apply forward bias, connect +ve terminal of the battery to p-type and –ve terminal to n-type as shown in fig.2.1 below.

- The applied forward potential(V_F) establishes the electric field which acts against the field due to potential barrier. Therefore the resultant field is weakened and the barrier height is reduced at the junction as shown in fig. 2.1.

- Since the potential barrier voltage is very small, a small forward voltage(V_F) is sufficient to completely eliminate the barrier. Once the potential barrier is eliminated by the forward voltage, junction resistance (R_F) becomes almost zero and a low resistance path is established for the entire circuit. Therefore current flows in the circuit. This is called forward current (I_F).

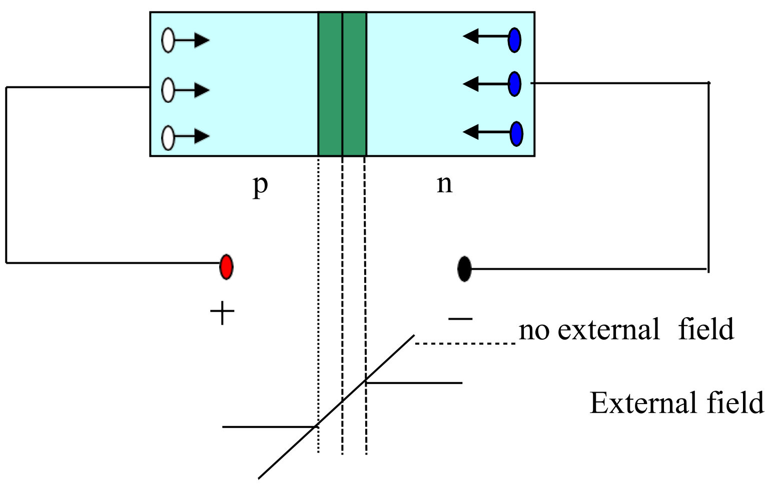


Figure 1.10: Forward biasing of p-n junction

2. Reverse biasing

- When the external voltage applied to the junction is in such a direction the potential barrier is increased it is called reverse biasing.

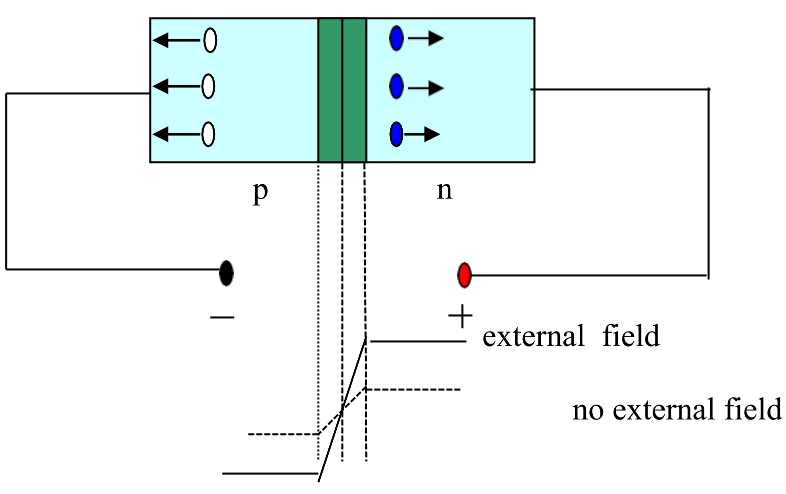


Figure 1.11: Reverse biasing of p-n junction

- To apply reverse bias, connect –ve terminal of the battery to p-type and +ve terminal to n-type as shown in figure below.

- The applied reverse voltage establishes an electric field which acts in the same direction as the field due to potential barrier. Therefore the resultant field at the junction is strengthened and the barrier height is increased as shown in fig.2.2.

- The increased potential barrier prevents the flow of charge carriers across the junction. Thus a high resistance path (R_R) is established for the entire circuit and hence current does not flow. But in practice a very little current flows due to minority charge carriers. The current is called reverse saturation current (I_S).

Volt- Ampere characteristics (V-I) of a PN junction diode:

1. **Forward Bias -** The voltage potential is connected positive, (+ve) to the P-type material and negative, (-ve) to the N-type material across the diode which has the effect of **Decreasing** the PN-junction width.

2. **Reverse Bias** - The voltage potential is connected negative, (-ve) to the P-type material and positive, (+ve) to the N-type material across the diode which has the effect of **Increasing** the PN-junction width

Forward Biased Junction Diode:

When a diode is connected in a **Forward Bias** condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material.

If this external voltage (V_F) becomes greater than the value of the potential barrier (V_γ), approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This current is called forward current(I_F)

This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage.

This results in a characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

Forward Characteristics:

Case 1:

When the applied forward voltage $V_F < V_\gamma$, the width of the depletion layer is increased and no current flows through the circuit.

Case 2:

When the applied forward voltage $V_F > V_\gamma$, the charge carriers move towards the junction from P to N and from N to P, due to this the width of the junction gets reduced and at one particular voltage the junction gets damaged ,and forward resistance(R_F) offered by the diode will be very less (ideally 0) due to this there will be a flow of current due to majority charge carriers. The current is said to be forward current (I_F) which will be very large.

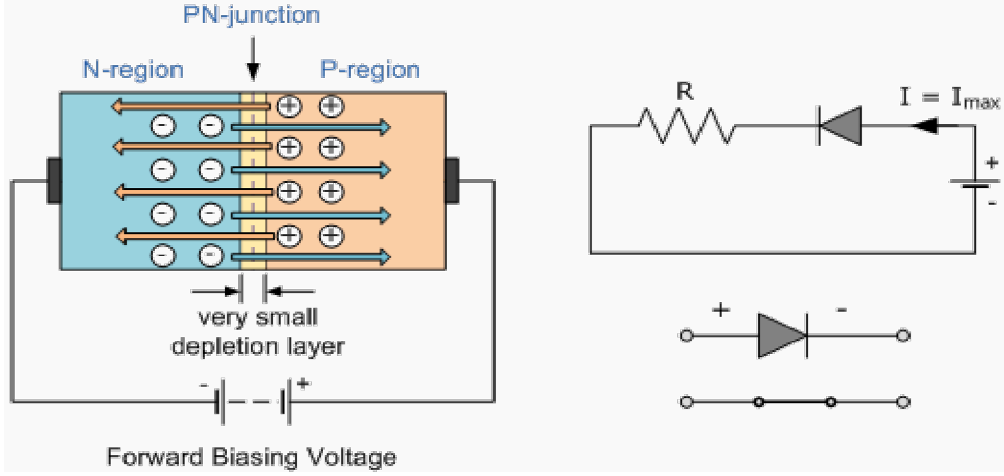


Figure 1.12: Forward Biased Junction Diode showing a Reduction in the Depletion Layer

This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes. Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow.

Reverse Biased Junction Diode:

When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material.

The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode.

The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

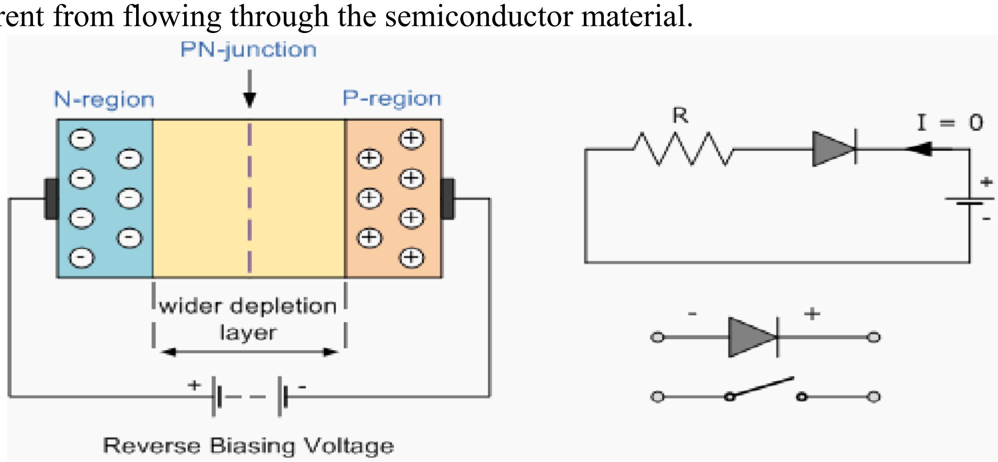


Figure 1.13: Reverse Biased Junction Diode showing an Increase in the Depletion Layer

This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current (I_S)** does flow through the junction which can be measured in microamperes, (μA). One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will cause the PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current and this shown as a step downward slope in the reverse static characteristics curve below.

Sometimes this avalanche effect has practical applications in voltage stabilising circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset maximum value thereby producing a fixed voltage output across the diode. These types of diodes are commonly known as **Zener Diodes**.

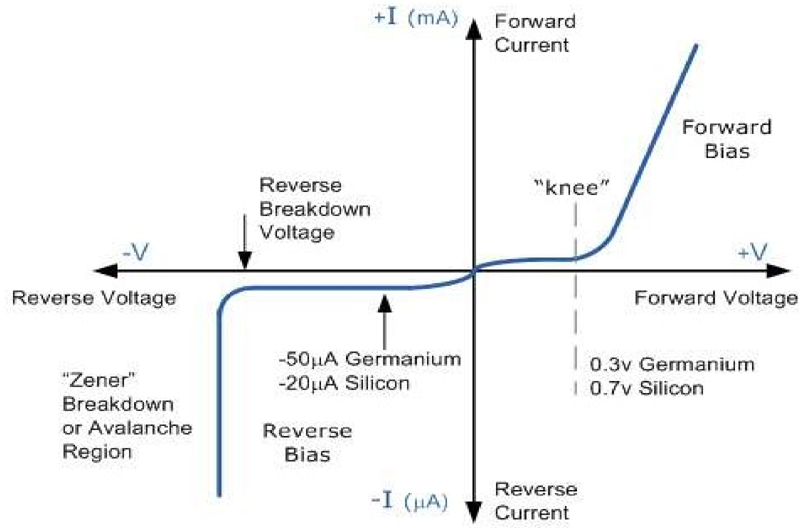


Figure 1.14: V-I Characteristics of PN Junction Diode

<u>PN diode Currents:</u>

The expression for the total current as a function of the applied voltage is derived below.

Here we neglect the depletion layer thickness and hence assume that the barrier width is 0. If a forward bias is applied to the diode, the holes are injected from P side to n material. The concentration of holes in the side is increased above its thermal equilibrium value P_n and given by ,

$$P_n(x) = P_{no} + P_{n(o)} e^{-x/LP} \quad \text{-------- (1)}$$

Where,

L_P is called the diffusion length for holes in 'n' material and the injected or excess concentration at X = 0 is

$$P_n(o) = P_n(o) - P_{no} \ldots\ldots (2)$$

These several hole concentration components are indicated in figure which shows the exponential decrease of the density $P_n(x)$ with distance X into the n material.

The diffusion hole concentration components are indicated, in figure, which shows the exponential decrease the density $P_n(x)$ with distance x into the n material. The diffusion hole current in the n side is given by

$$ipn = - Ae \frac{D_P d_{pn}}{dp_x} \quad \ldots(3)$$

Sub (1) in (3) we obtain

$$ip_n(x) = \frac{A_e D_P P_n(o) e^{-x/LP}}{L_P} \quad \ldots\ldots\ldots (4)$$

This equation verifies that the hole current decreases exponentially with distance. The dependence of Ipn up to applied voltage is contained implicitly in the factor P_n (o) because the injected concentration is a function of voltage. We now find the dependence of $P_n(o)$ upon V.

Law of junction:

If the hole concentration at the edges of space charge region as P_n and P_P in the P and n materials, respectively and if the barrier potential across this depletion layer V_B, then

$$P_P = P_n e^{V_B/V_T} \text{.......... (5)}$$

This is the Boltzmann relationship of kinetic gas theory. If we apply equation (5) to the case of an open Cktd on junction, then

$P_p = P_{PO}$, $P_n = O_{no}$ and $V_B = V_o$.

At the edge of depletion layer X = 0, $P_n = P_n(o)$.

The Boltzmann relation, i.e for this case.

$$P_{PO} = P_n(O)e^{(V_0 - V)/V_T} \text{.......... (6)}$$

Combining this equation with $V_0/V_T = E_0/KT$.

$$P_n(O) = P_{no}e^{V/V_T} \text{.......... (7)}$$

This boundary condition is called the law of junction.

The hole concentration P_n (O) injected into n side at the junction is obtained by subs equation (6) in equation (2)

$$P_n(O) = P_nO\left(e^{V/V_T} - 1\right) \text{ (8)}$$

The Forward Currents:-

The hole current IPn(O) crossing the junction into n side is given by equation (4) we obtain

$$IPn(O) = \frac{A_e D_P P_{no}}{L_P}(e^{V/V_T} - 1) \text{....... (9)}$$

The election current InP (O) crossing junction into P side is obtained from equation 9 by interchanging n & P or

$$InP(O) = \frac{A_e D_P n_{po}}{L_n}(e^{V/V_T} - 1) \text{....... (10)}$$

Total diode current is given by

$$I = I_{Pn}(O) + I_{NP}(O)$$

$$I = I_O\left(e^{V/V_T} - 1\right)$$

Temperature dependence of V-I characteristics of p-n junction diode:

The temperature has following effects on the diode parameters,

1. The cut-in voltage decreases as the temperature increases. The diode conducts at smaller voltage at large temperature.
2. The reverse saturation current increases as temperature increases.

This increases in reverse current I_o is such that it doubles at every 10 ºC rise in temperature. Mathematically,

$$I_{o2} = 2^{(\Delta T/10)} I_{o1}$$

where I_{o2} = Reverse current at T_2 ºC

I_{o1} = Reverse current at T_1 C

$\Delta T = (T_2 - T_1)$

3. The voltage equivalent of temperature V_T also increases as temperature increases.
4. The reverse breakdown voltage increases as temperature increases as shown.

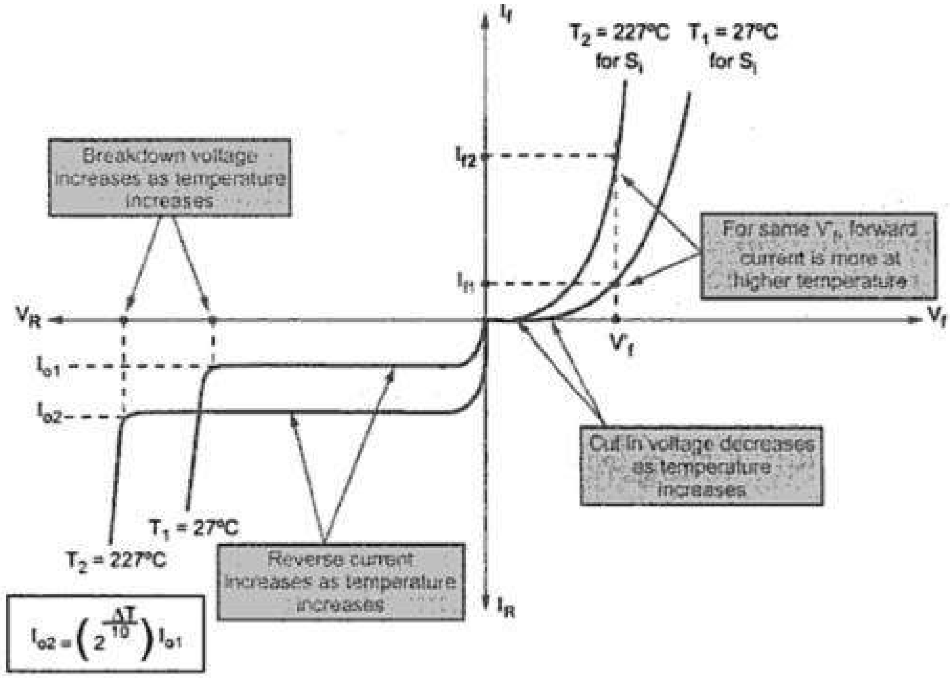


Figure 1.15: Effect of Temperature on PN Diode characteristics

(a) Effect of Temperature on forward voltage drop:

Most of the times, the drop across the diode is assumed constant. But in few situations, it is necessary to consider the effect of temperature on forward voltage drop.

It is seen that cut-in voltage decreases as temperature increases.

Note :The diode forward voltage drop decrease as temperature increases.

The rate at which it increases is - 2.3 mV/ ºC for silicon while - 2.12 mV/ ºC for germanium. The negative sign shows decrease in forward voltage drop as temperature increases. This is shown in figure below.

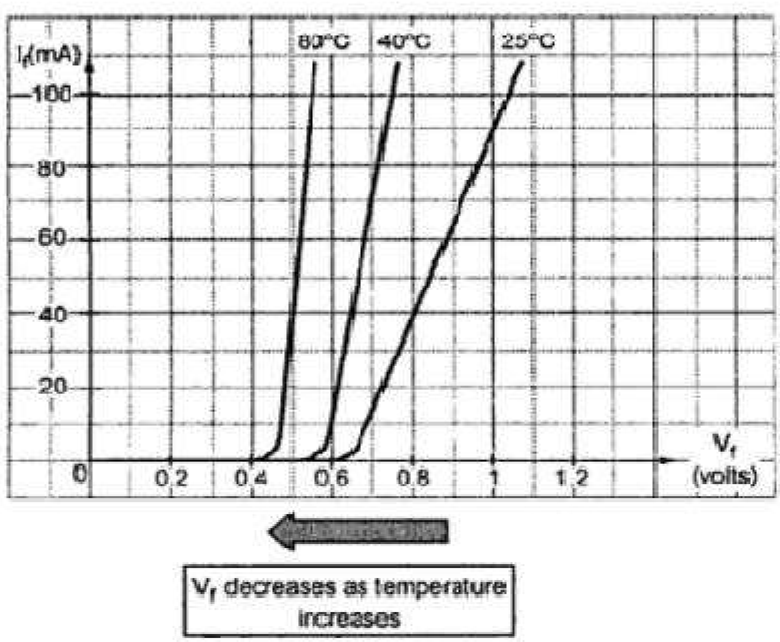


Figure 1.15: Effect of Temperature on forward voltage drop

The coefficient ΔV_f/ °C is called voltage/temperature coefficient of diode. Knowing this and V_{f1} at T_1, any V_{f2} at T_2 can be obtained as,

$$\boxed{V_{f_2} = V_{f1} + [\Delta T \times \text{Voltage / temperature coefficient}]} \quad \ldots (4)$$

(b) <u>Effect of Temperature on Dynamic Resistance:</u>

The dynamic resistance of the diode is obtained as,

$$r_f' = \frac{26\ \text{mV}}{I_f} = \frac{V_T}{I_f} = \frac{kT}{I_f}$$

where k = Boltzman's constant and T in °K constant.

The value 26 mV is temperature dependent and the above equation is applicable only at 25 °C. For higher temperatures, it gets changed as,

$$\boxed{r_f' = \frac{kT'}{I_f}} \quad \ldots (5)$$

where T' is new temperature in °K.

The above equation can be expressed as,

$$\boxed{r_f' = \frac{26\ \text{mV}}{I_f}\left[\frac{T'\ \text{in}\ °\text{K}}{298\ °\text{C}}\right]} \quad \ldots (6)$$

Note : As temperature increases, V_T increase hence dynamic forward resistance increases.

<u>Diode Junction capacitance:</u>

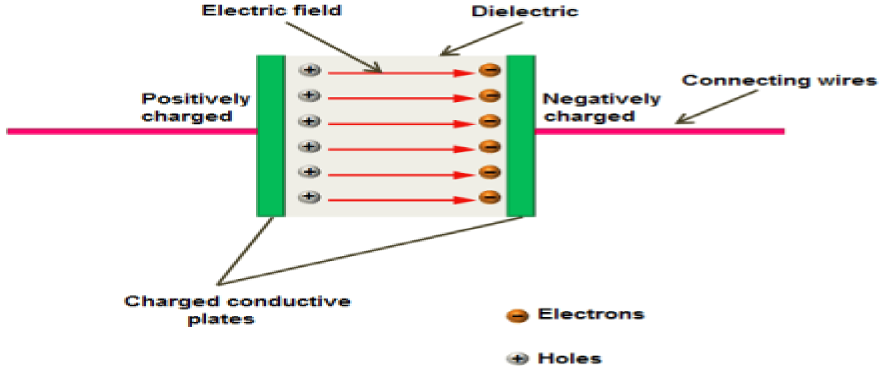
In a p-n junction diode, two types of capacitance take place. They are,

- Transition capacitance (C_T)
- Diffusion capacitance (C_D)

<u>(a) Transition capacitance (C_T):</u>

We know that capacitors store electric charge in the form of electric field. This charge storage is done by using two electrically conducting plates (placed close to each other) separated by an insulating material called dielectric.

The conducting plates or electrodes of the capacitor are good conductors of electricity. Therefore, they easily allow electric current through them. On the other hand, dielectric material or medium is poor conductor of electricity. Therefore, it does not allow electric current through it. However, it efficiently allows electric field.



When voltage is applied to the capacitor, charge carriers starts flowing through the conducting wire. When these charge carriers reach the electrodes of the capacitor, they experience a strong opposition from the dielectric or insulating material. As a result, a large number of charge carriers are trapped at the electrodes of the capacitor. These charge carriers cannot move between the plates. However, they exerts electric field between the plates. The charge carriers which are trapped near the dielectric material will stores electric charge. The ability of the material to store electric charge is called capacitance.

In a basic capacitor, the capacitance is directly proportional to the size of electrodes or plates and inversely proportional to the distance between two plates.

Just like the capacitors, a reverse biased p-n junction diode also stores electric charge at the depletion region. The depletion region is made of immobile positive and negative ions.

In a reverse biased p-n junction diode, the p-type and n-type regions have low resistance. Hence, p-type and n-type regions act like the electrodes or conducting plates of the capacitor. The depletion region of the p-n junction diode has high resistance. Hence, the depletion region acts like the dielectric or insulating material. Thus, p-n junction diode can be considered as a parallel plate capacitor.

In depletion region, the electric charges (positive and negative ions) do not move from one place to another place. However, they exert electric field or electric force. Therefore, charge is stored at the depletion region in the form of electric field. The ability of a material to store electric charge is called capacitance. Thus, there exists a capacitance at the depletion region.

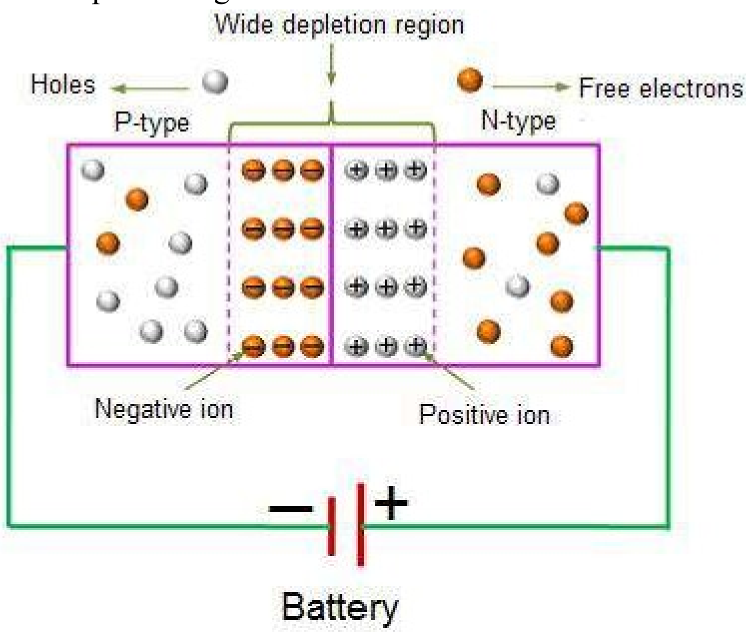


Figure 1.16: Transition Capacitance

The capacitance at the depletion region changes with the change in applied voltage. When reverse bias voltage applied to the p-n junction diode is increased, a large number of holes(majority carriers) from p-side and electrons (majority carriers) from n-side are moved away from the p-n junction. As a result, the width of depletion region increases whereas the size of p-type and n-type regions (plates) decreases.

We know that capacitance means the ability to store electric charge. The p-n junction diode with narrow depletion width and large p-type and n-type regions will store large amount of electric charge whereas the p-n junction diode with wide depletion width and small p-type and n-type regions will store only a small amount of electric charge. Therefore, the capacitance of the reverse bias p-n junction diode decreases when voltage increases.

In a forward biased diode, the transition capacitance exist. However, the transition capacitance is very small compared to the diffusion capacitance. Hence, transition capacitance is neglected in forward biased diode.

The amount of capacitance changed with increase in voltage is called transition capacitance. The transition capacitance is also known as depletion region capacitance, junction capacitance or barrier capacitance. Transition capacitance is denoted as C_T.

The change of capacitance at the depletion region can be defined as the change in electric charge per change in voltage.

$$C_T = dQ / dV$$

Where,

C_T = Transition capacitance

dQ = Change in electric charge

dV = Change in voltage

The transition capacitance can be mathematically written as,

$$C_T = \varepsilon A / W$$

Where,

ε = Permittivity of the semiconductor

A = Area of plates or p-type and n-type regions

W = Width of depletion region

Diffusion capacitance (C_D):

Diffusion capacitance occurs in a forward biased p-n junction diode. Diffusion capacitance is also sometimes referred as storage capacitance. It is denoted as C_D.

In a forward biased diode, diffusion capacitance is much larger than the transition capacitance. Hence, diffusion capacitance is considered in forward biased diode.

The diffusion capacitance occurs due to stored charge of minority electrons and minority holes near the depletion region.

When forward bias voltage is applied to the p-n junction diode, electrons (majority carriers) in the n-region will move into the p-region and recombines with the holes. In the similar way, holes in the p-region will move into the n-region and recombines with electrons. As a result, the width of depletion region decreases.

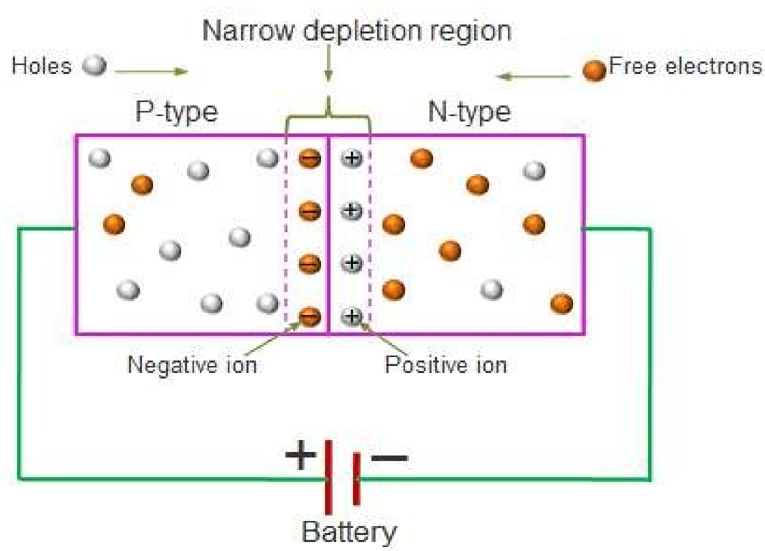


Figure 1.17: Diffusion Capacitance

The electrons (majority carriers) which cross the depletion region and enter into the p-region will become minority carriers of the p-region similarly; the holes (majority carriers) which cross the depletion region and enter into the n-region will become minority carriers of the n-region.

A large number of charge carriers, which try to move into another region will be accumulated near the depletion region before they recombine with the majority carriers. As a result, a large amount of charge is stored at both sides of the depletion region.

The accumulation of holes in the n-region and electrons in the p-region is separated by a very thin depletion region or depletion layer. This depletion region acts like dielectric or insulator of the capacitor and charge stored at both sides of the depletion layer acts like conducting plates of the capacitor.

Diffusion capacitance is directly proportional to the electric current or applied voltage. If large electric current flows through the diode, a large amount of charge is accumulated near the depletion layer. As a result, large diffusion capacitance occurs.

In the similar way, if small electric current flows through the diode, only a small amount of charge is accumulated near the depletion layer. As a result, small diffusion capacitance occurs.

When the width of depletion region decreases, the diffusion capacitance increases. The diffusion capacitance value will be in the range of nano farads (nF) to micro farads (μF).

The formula for diffusion capacitance is

$$C_D = dQ / dV$$

Where,

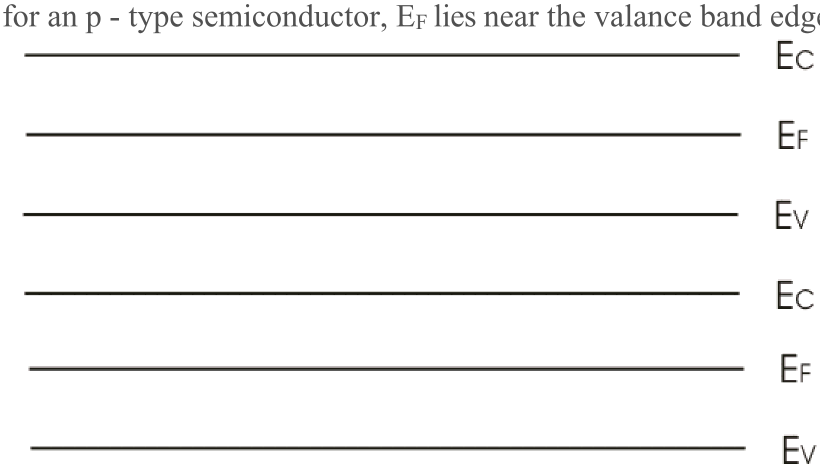
C_D = Diffusion capacitance

dQ = Change in number of minority carriers stored outside the depletion region

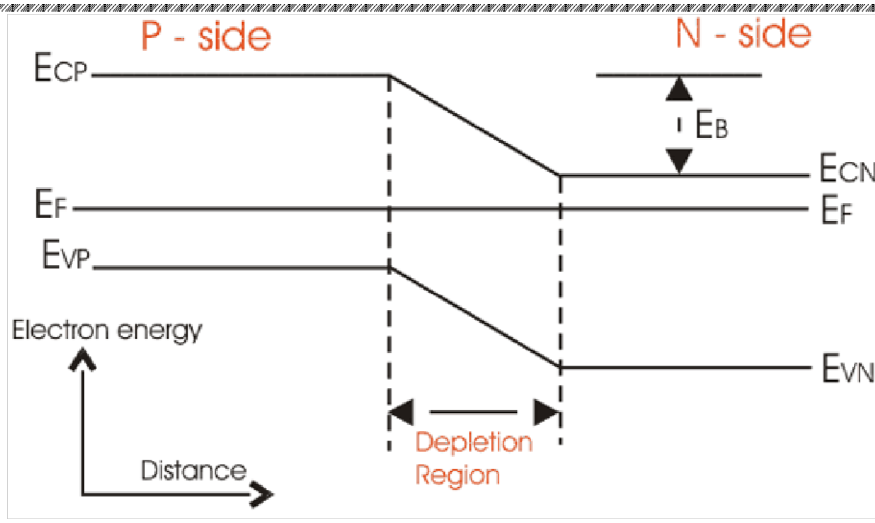
dV = Change in voltage applied across diode

Energy Band Diagram of P-N Diode:

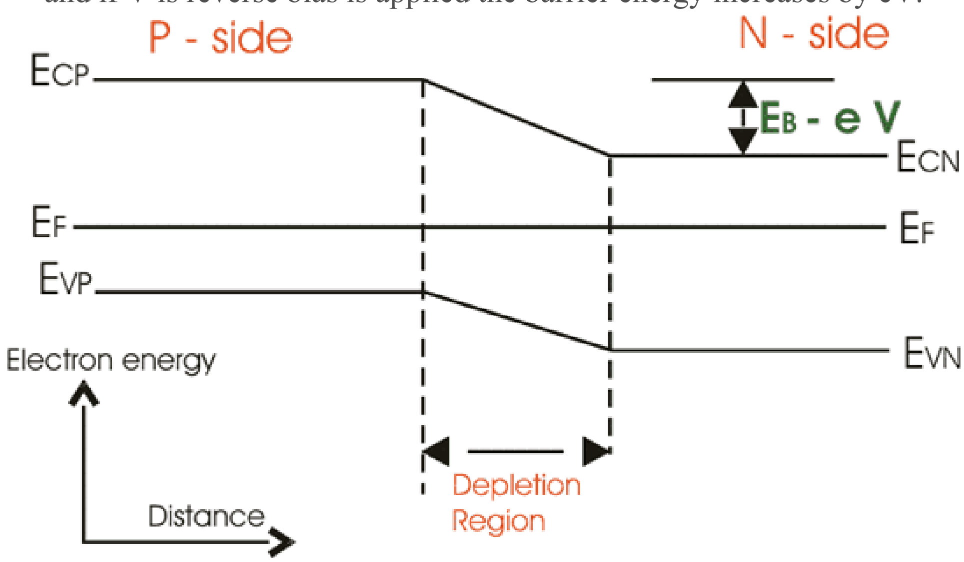
For an n-type semiconductor, the Fermi level E_F lies near the conduction band edge. E_C but for an p - type semiconductor, E_F lies near the valance band edge E_V.

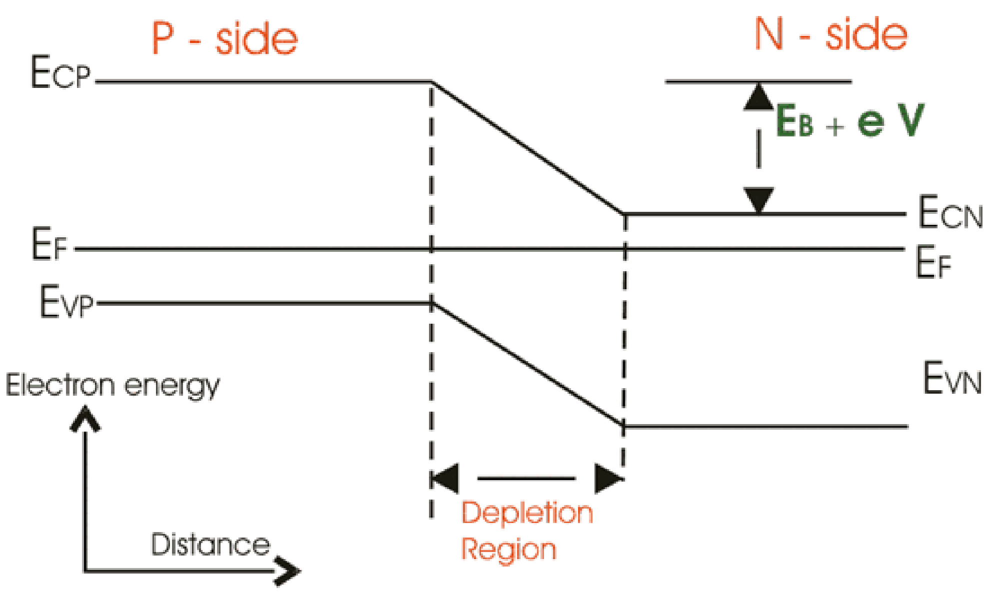


Now, when a p-n junction is built, the Fermi energy E_F attains a constant value. In this scenario the p-sides conduction band edge. Similarly n–side valance band edge will be at higher level than E_{cn}, n-sides conduction band edge of p - side. This energy difference is known as barrier energy. The barrier energy is $E_B = E_{cp} - E_{cn} = E_{vp} - E_{vn}$



If we apply forward bias voltage V, across junction then the barrier energy decreases by an amount of eV and if V is reverse bias is applied the barrier energy increases by eV.





Static and Dynamic Resistances:

(a) DC or Static Resistance :

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the Corresponding levels of V_D and I_D as shown in Fig. 1.18 and applying the following Equation:

$$\boxed{R_D = \frac{V_D}{I_D}}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

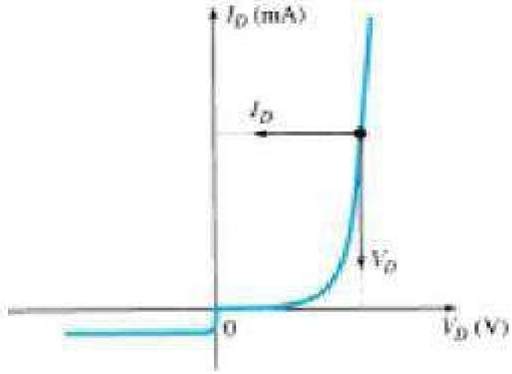


Figure 1.18: Determining the dc resistance of a diode at a particular operating point

(b) AC or Dynamic Resistance :

It is obvious from the above equation of static resistance that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely.

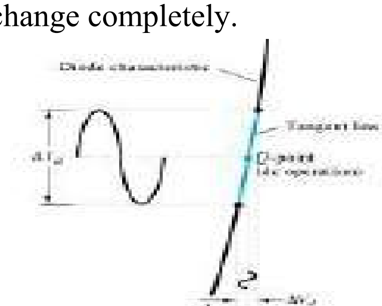


Figure 1.19: Defining the ac resistance of a diode

The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.19. With no applied varying signal, the point of operation would be the *Q*-point appearing on Fig. 1.19 determined by the applied dc levels. The designation *Q-point* is derived from the word *quiescent,* which means —still or unvarying.

A straight line drawn tangent to the curve through the *Q*-point as shown in Fig. 1.20 will define a particular change in voltage and current that can be used to determine the *ac* or *dynamic* resistance for this region of the diode characteristics. In equation form,

$$\boxed{r_d = \frac{\Delta V_d}{\Delta I_d}}$$

Figure 1.20: Determining the ac resistance of a diode at Q point

<u>Diode Equivalent Circuits:</u>

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region. In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behavior of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

<u>(a)</u> <u>Piecewise-Linear Equivalent Circuit :</u>

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.21. The resulting equivalent circuit is naturally called the *piecewise-linear equivalent circuit.* It should be obvious from Fig. 1.21 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behavior of the device. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open circuit state for the device. Since a silicon semiconductor diode does not reach the conduction state until V_D reaches 0.7 V with a forward bias (as shown in Fig. 1.21), a battery V_T opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.21. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established the resistance of the diode will be the specified value of $r_{av.}$

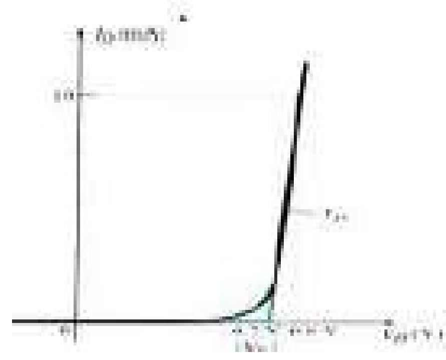


Figure 1.21: Defining the piecewise-linear equivalent circuit using straight-line segments to approximate the characteristic curve

The approximate level of *rav* can usually be determined from a specified operating point on the specification sheet. For instance, for a silicon semiconductor diode, if I_F =10 mA (a forward conduction current for the diode) at V_D = 0.8 V, we know for silicon that a shift of 0.7 V is required before the characteristics rise.

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}} = \frac{0.8\text{ V} - 0.7\text{ V}}{10\text{ mA} - 0\text{ mA}} = \frac{0.1\text{ V}}{10\text{ mA}} = \mathbf{10\ \Omega}$$

(b) Simplified Equivalent Circuits :

For most applications, the resistance r_{av} is sufficiently small to be ignored in comparison to the other elements of the network. The removal of r_{av} from the equivalent circuit is the same as implying that the characteristics of the diode. Under dc conditions has a drop of 0.7 V across it in the conduction state at any level of diode current.

(c) Ideal Equivalent Circuits:

Now that r_{av} has been removed from the equivalent circuit let us take it a step further and establish that a 0.7-V level can often be ignored in comparison to the applied voltage level. In this case the equivalent circuit will be reduced to that of an ideal diode as shown in Fig. 1.22 with its characteristics.

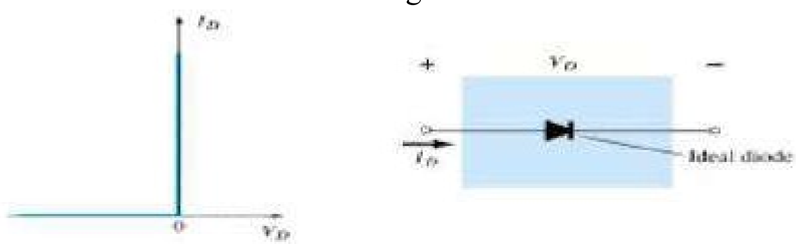


Figure 1.22: Ideal diode and its characteristics

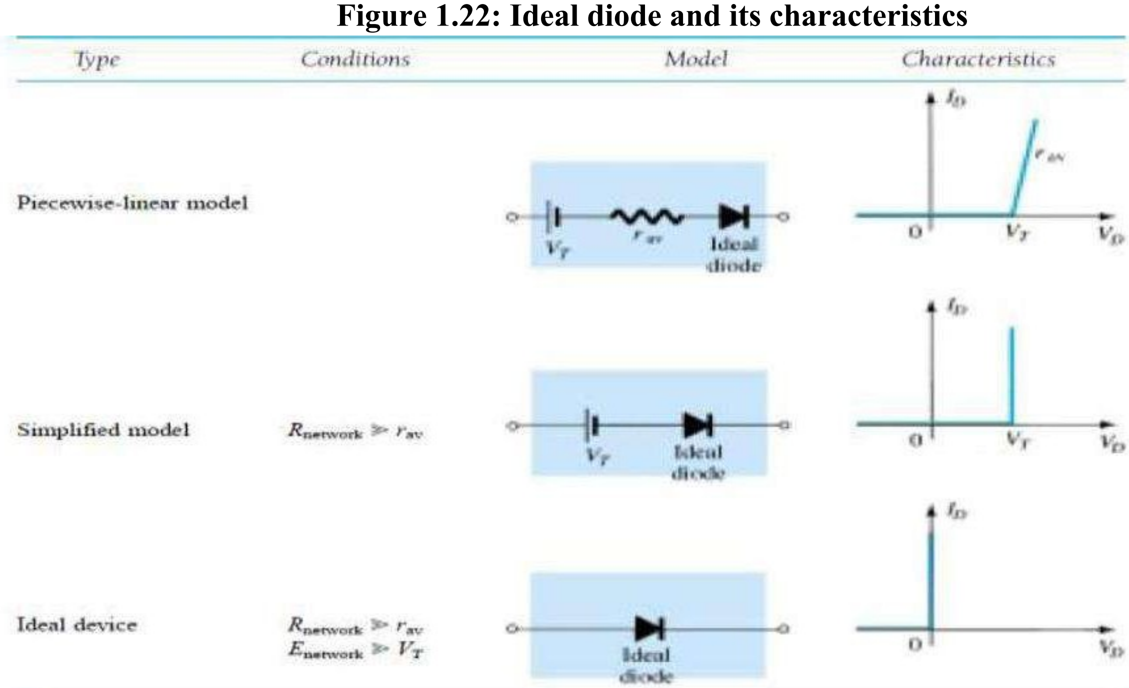


Figure 1.23: Diode equivalent circuits

Rectifiers and Filters:

Introduction:

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c. voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification.This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.

These elements constitute d.c. regulated power supply shown in the figure below.

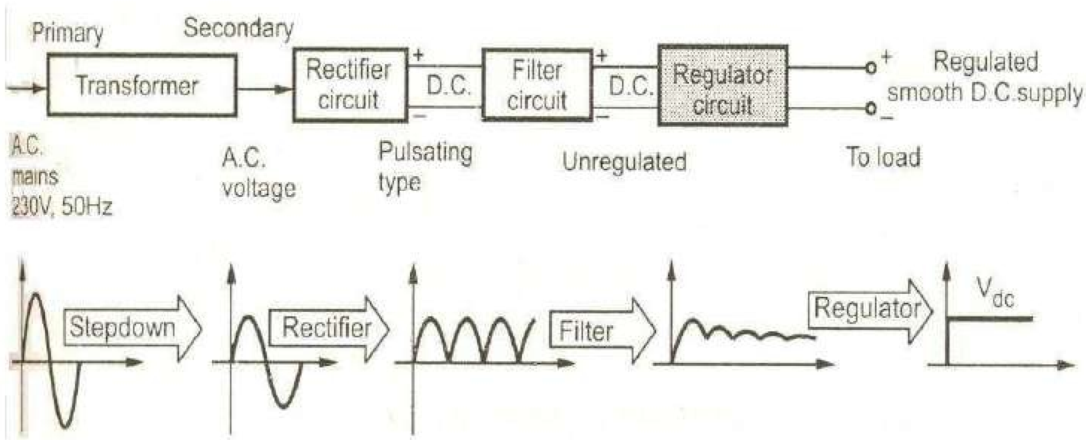


Fig. Block diagram of Regulated D.C. Power Supply

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load.

An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage Vo which is independent of the load current and variations in the input voltage ad temperature.

If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

The elements of the regulated DC power supply are discussed as follows:

TRANSFORMER:

A transformer is a static device which transfers the energy from primary winding to secondary winding through the mutual induction principle, without changing the frequency. The transformer winding to which the supply source is connected is called the primary, while the winding connected to the load is called secondary.

If N_1,N_2 are the number of turns of the primary and secondary of the transformer then $\alpha = \frac{N_2}{N_1}$ is called the turns ratio of the transformer.

The different types of the transformers are

- Step-Up Transformer
- Step-Down Transformer
- Centre-tapped Transformer

The voltage, current and impedance transformation ratios are related to the turns ratio of the transformer by the following expressions.

Voltage transformation ratio : $\frac{V_2}{V_1} = \frac{N_2}{N_1}$

Current transformation ratio : $\frac{I_2}{I_1} = \frac{N_1}{N_2}$

Impedance transformation ratio : $\frac{Z_L}{Z_{in}} = \left(\frac{N_2}{N_1}\right)^2$

RECTIFIER:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component.

A rectifier is a device which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Uni-directional).

Important characteristics of a Rectifier Circuit:

1. **Load currents:** They are two types of output current. They are average or d.c. current and RMS currents.

   i) **Average or DC current:** The average current of a periodic function is defined as the area of one cycle of the curve divided by the base.

   It is expressed mathematically as $I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} id(\omega t)$; where $i = I_m \sin \omega t$

   6) **Effective (or) R.M.S. current:** The effective (or) R.M.S. current squared of a periodic function of time is given by the area of one cycle of the curve which represents the square of the function divided by the base.

   It is expressed mathematically as $I_{rms} = \left[\frac{1}{2\pi} \int_0^{2\pi} i^2 d(\omega t) \right]^{\frac{1}{2}}$

2. **Load Voltages:** There are two types of output voltages. They are average or D.C. voltage and R.M.S. voltage.

   i) **Average or DC Voltage:** The average voltage of a periodic function is defined as the areas of one cycle of the curve divided by the base.
   It is expressed mathematically as

   $$V_{dc} = \frac{1}{2\pi} \int_0^{2\pi} Vd(\omega t) \text{ ; Where } V = V_m \sin \omega t$$

   (or) $V_{dc} = I_{dc} \times R_L$

   ii) **Effective (or) R.M.S Voltage:** The effective (or) R.M.S voltage squared of a periodic function of time is given by the area of one cycle of the curve which represents the square of the function divided by the base.

$$V_{rms} = \left[\frac{1}{2\pi} \int_0^{2\pi} V^2 d(\omega t) \right]^{\frac{1}{2}} \qquad V_{rms} = I_{rms} \times R_L$$

3. **Ripple Factor (γ) :** It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

$$\gamma = \frac{V_{rms}}{V_{dc}}$$

$$V_{rms} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\therefore \gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

4. **Efficiency (η) :** It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

It is given by $$\eta = \frac{P_{dc}}{P_{Ac}}$$

5. **Peak Inverse Voltage (PIV):** It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction.

6. **Regulation:** The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\% \text{ Regulation} = \frac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100\%$$

For an ideal power supply, % Regulation is zero.

Using one or more diodes in the circuit, following rectifier circuits can be designed.

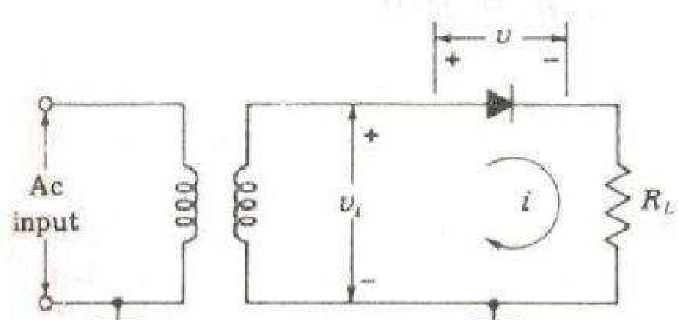
1. Half - Wave Rectifier
2. Full – Wave Rectifier
3. Bridge Rectifier

HALF-WAVE RECTIFIER:

A Half – wave rectifier is one which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage. The basic half-wave diode rectifier circuit along with its input and output waveforms is shown in figure below.

The half-wave rectifier circuit shown in above figure consists of a resistive load; a rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer.

The input to the rectifier circuit, $V = V_m \sin \omega t$ Where Vm is the peak value of secondary a.c. voltage



(a)

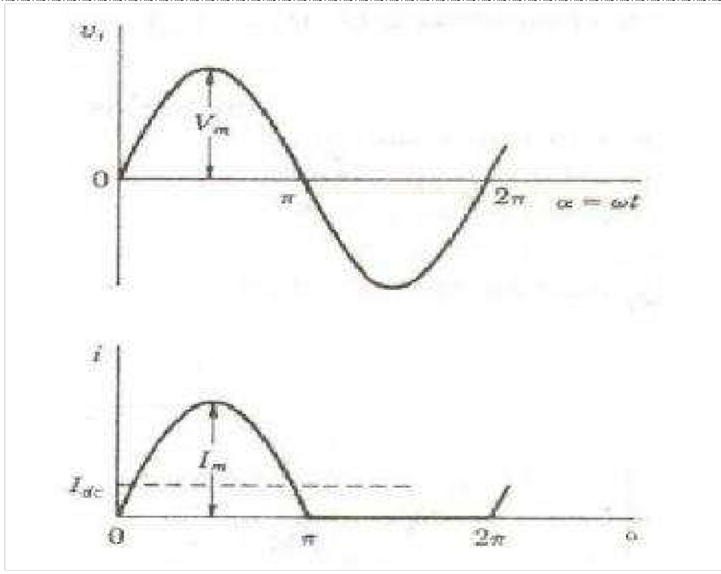


Figure 1.24: Circuit and Waveforms of half wave rectifier

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across R_L. The waveform of the diode current (or) load current is shown in figure.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half-cycle no power is delivered to the load.

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

i) DC output current
ii) DC Output voltage
iii) R.M.S. Current
iv) R.M.S. voltage
v) Rectifier Efficiency (η)
vi) Ripple factor (γ)
vii) Regulation
viii) Transformer Utilization Factor (TUF)
ix) Peak Factor (P)

Let a sinusoidal voltage V_i be applied to the input of the rectifier.

Then $V = V_m \sin \omega t$ Where Vm is the maximum value of the secondary voltage.

Let the diode be idealized to piece-wise linear approximation with resistance R_f in the forward direction i.e., in the ON state and R_r (=∞) in the reverse direction i.e., in the OFF state.

Now the current 'i' in the diode (or) in the load resistance R_L is given by

$$i = I_m \sin \omega t \quad \text{for} \quad 0 \le \omega t \le \pi$$

$$i = 0 \quad \text{for} \quad \pi \le \omega t \le 2\pi$$

$$\text{where } I_m = \frac{V_m}{R_f + R_L}$$

i) Average (or) DC Output Current (I_{av} or I_{dc}):

The average dc current I_{dc} is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i\,d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t\,d(\omega t) + \int_{\pi}^{2\pi} 0 \times d(\omega t)$$

$$= \frac{1}{2\pi} I_m (-\cos\omega t)_0^{\pi}$$

$$= \frac{1}{2\pi} I_m (+1-(-1))$$

$$= \frac{I_m}{\pi} = 0.318\, I_m$$

Substituting the value of I_m, we get $I_{dc} = \dfrac{V_m}{\pi(R_f + R_L)}$

If $R_L >> R_f$ then $I_{dc} = \dfrac{V_m}{\pi R_L} = 0.318\dfrac{V_m}{R_L}$

ii) Average (or) DC Output Voltage (V_{av} or V_{dc}):

The average dc voltage is given by

$$V_{dc} = I_{dc} \times R_L = \frac{I_m}{\pi} \times R_L = \frac{V_m R_L}{\pi(R_f + R_L)}$$

$$\Rightarrow V_{dc} = \frac{V_m R_L}{\pi(R_f + R_L)}$$

If $R_L >> R_f$ then $V_{dc} = \dfrac{V_m}{\pi} = 0.318\, I_m$ $\quad \therefore V_{dc} = \dfrac{V_m}{\pi}$

iii) RMS output current (I_{rms}):

The value of the R.M.S. current is given by

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} i^2 d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\omega t . d(\omega t) + \frac{1}{2\pi}\int_{\pi}^{2\pi} . 0 . d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{2\pi}\int_0^{\pi}\frac{1-\cos\omega t}{2}\,d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi}\left[(\omega t) - \frac{1}{2}\sin\omega t\right]_0^{\pi}\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi}\left(\pi - 0 - \frac{\sin 2\pi}{2} + \frac{\sin 0}{2}\right)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4}\right]^{\frac{1}{2}} = \frac{I_m}{2}$$

$$\therefore I_{rms} = \frac{I_m}{2} \qquad I_{rms} = \frac{V_m}{2(R_f + R_L)}$$

iv) R.M.S. Output Voltage (V_{rms}):

R.M.S. voltage across the load is given by

$$V_{rms} = I_{rms} \times R_L = \frac{V_m R_L}{2(R_f + R_L)} = \frac{V_m}{2\left(1 + \frac{R_f}{R_L}\right)}$$

If $R_L >> R_f$ then $V_{rms} = \frac{V_m}{2}$

v) Rectifier efficiency(η) :

The rectifier efficiency is defined as the ration of d.c. output power to the a.c. input power i.e.,

$$\eta = P_{dc}/P_{ac}$$

Theoretically the maximum value of rectifier efficiency of a half-wave rectifier is 40.6%

vi) Ripple Factor (γ) :

The ripple factor γ is given by

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \quad \text{(or)} \quad \gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$\therefore \gamma = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

$$\Rightarrow \gamma = 1.21$$

vii) Regulation:

The variation of d.c. output voltage as a function of d.c. load current is called *regulation.*

The variation of V_{dc} with I_{dc} for a half-wave rectifier is obtained as follows:

$$I_{dc} = \frac{I_m}{\pi} = \frac{V_m/\pi}{R_f + R_L}$$

But $V_{dc} = I_{dc} \times R_L$

$$V_{dc} = \frac{V_m}{\pi} \frac{R_L}{R_f + R_L} = \frac{V_m}{\pi}\left(1 - \frac{R_f}{R_f + R_L}\right)$$

$$= \frac{V_m}{\pi} - I_{dc} R_f$$

$$\therefore V_{dc} = \frac{V_m}{\pi} - I_{dc} R_f$$

This result shows that V_{dc} equals π at no load and that the dc voltage decreases linearly with an increase in dc output current. The larger the magnitude of the diode forward resistance, the greater is this decrease for a given current change.

viii) Transformer Utilization Factor (UTF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$\therefore TUF = \frac{P_{dc}}{P_{ac\,(rated)}}$$

The factor which indicates how much is the utilization of the transformer in the circuit is called Transformer Utilization Factor (TUF).

The a.c. power rating of transformer $= V_{rms} I_{rms}$

The secondary voltage is purely sinusoidal hence its rms value is $\frac{1}{\sqrt{2}}$ times maximum while the current is half sinusoidal hence its rms value is $\frac{1}{2}$ of the maximum.

$$\therefore P_{ac\,(rated)} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{2} = \frac{V_m I_m}{2\sqrt{2}}$$

The d.c. power delivered to the load $= I_{dc}^2 R_L = \left(\frac{I_m}{\pi}\right)^2 R_L$

$$\therefore TUF = \frac{P_{dc}}{P_{ac\,(rated)}}$$

$$= \left(\frac{I_m}{\pi}\right)^2 R_L \times \frac{2\sqrt{2}}{V_m I_m}$$

$$= \frac{I_m^2 \cdot R_L \cdot 2\sqrt{2}}{\pi^2 \cdot I_m \cdot R_L} \qquad (\because V_m \approx I_m R_L)$$

= 0.287

$$\therefore TUF = 0.287$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized.

If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver 1000 X 0.287 = 287 watts to resistance load.

ix) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half-cycle. For half-wave rectifier, PIV is V_m.

x) Form factor (F):

The Form Factor F is defined as

F = rms value / average value

$$F = \frac{Im/2}{Im/\pi}$$

$$F = \frac{0.5\ Im}{0.318\ Im} = 1.57$$

xi) Peak Factor (P):

The peak factor P is defined as

P= Peak Value / rms value $= \dfrac{V_m}{V_m / 2} = 2$ **P = 2**

Disadvantages of Half-Wave Rectifier:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

Problems from previous external question paper:

1. A diode whose internal resistance is 20J is to supply power to a 100J load from 110V(rms) source pf supply. Calculate (a) peak load current (b) the dc load current (c) the ac load current (d) the percentage regulation from no load to full load.

Solution:

Given a half-wave rectifier circuit R_f=20J, R_L=100J

Given an ac source with rms voltage of 110V, therefore the maximum amplitude of sinusoidal input is given by

$$V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 110 = \mathbf{155.56V}.$$

(a) Peak load current : $I_m = \dfrac{V_m}{R_f + R_L} \Rightarrow I_m = \dfrac{155.56}{120} = \mathbf{1.29A}$

(b) The dc load current : $I_{dc} = \dfrac{I_m}{\pi} = \mathbf{0.41A}$

(c) The ac load current : $I_{rms} = \dfrac{I_m}{2} = \mathbf{0.645A}$

(d) $V_{no\text{-}load}$: $\dfrac{V_m}{\pi} = \dfrac{155.56}{\pi} = \mathbf{49.51\ V}$

$V_{full\text{-}load}$: $\dfrac{V_m}{\pi} - I_{dc} R_f = \mathbf{41.26\ V}$

% Regulation $= \dfrac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100 = \mathbf{19.97\%}$

2. A diode has an internal resistance of 20J and 1000J load from 110V(rms) source pf supply. Calculate (a) the efficiency of rectification (b) the percentage regulation from no load to full load.

Solution:

Given a half-wave rectifier circuit R_f=20J, R_L=1000J

Given an ac source with rms voltage of 110V, therefore the maximum amplitude of sinusoidal input is given by

$$V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 110 = 155.56V.$$

(a) % Efficiency (η) = $\dfrac{40.6}{1+\frac{20}{100}} = \dfrac{40.6}{1.02}$ = **39.8%.**

(b) Peak load current : $I_m = \dfrac{V_m}{R_f + R_L} = \dfrac{155.56}{1020} = 0.1525$ A

= **152.5 mA**

The dc load current : $I_{dc} = \dfrac{I_m}{\pi}$ = **48.54 mA**

$V_{no\text{-}load} = \dfrac{V_m}{\pi} = \dfrac{155.56}{\pi}$ = **49.51 V**

$V_{full\text{-}load} = \dfrac{V_m}{\pi} - I_{dc} R_f$ = **49.51 – (48.54 x10^{-3} x 20)**

= **49.51 – 0.97 = 48.54 V**

% Regulation = $\dfrac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100$

= $\dfrac{49.51 - 48.54}{48.54} \times 100$ = **1.94 %**

3. An a.c. supply of 230V is applied to a half-wave rectifier circuit through transformer of turns ration 5:1. Assume the diode is an ideal one. The load resistance is 300J.

Find (a) dc output voltage (b) PIV (c) maximum, and (d) average values of power delivered to the load.

Solution: (a) The transformer secondary voltage = 230/5 = 46V.

Maximum value of secondary voltage, $V_m = \sqrt{2}$ x 46 = 65V.

Therefore, dc output voltage, $V_{dc} = \dfrac{V_m}{\pi} = \dfrac{65}{\pi}$ = **20.7 V**

(b) PIV of a diode : V_m = **65V**

(c) Maximum value of load current, $I_m = \dfrac{V_m}{R_L} = \dfrac{65}{300}$ = **0.217 A**

Therefore, maximum value of power delivered to the load,

$\mathbf{P_m} = I_m^2 \times R_L = (0.217)^2 \times 300$ = **14.1W**

(d) The average value of load current, $I_{dc} = \dfrac{V_{dc}}{R_L} = \dfrac{20.7}{300}$ = **0.069A**

Therefore, average value of power delivered to the load,

$\mathbf{P_{dc}} = I_{dc}^2 \times R_L = (0.069)^2 \times 300$ = **1.43W**

FULL – WAVE RECTIFIER

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center-tap transformer.

A center-tap transformer is the one which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the figure below.

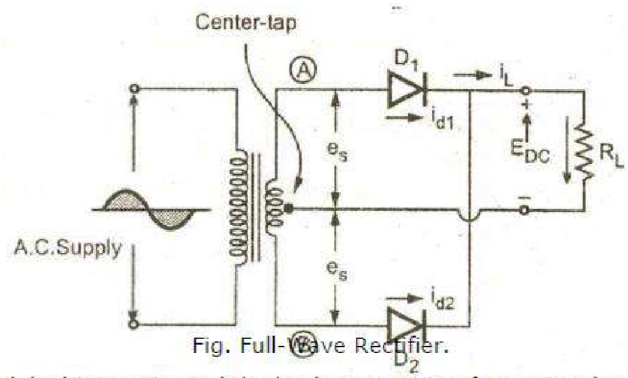


Fig. Full-Wave Rectifier.

The individual diode currents and the load current waveforms are shown in figure below:

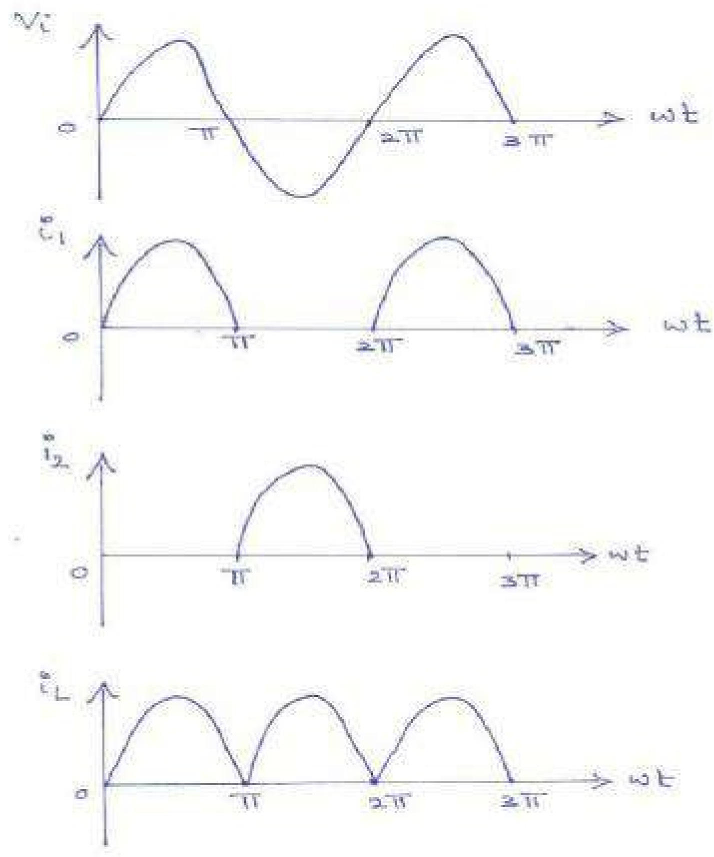


Figure 1.25: Input & Output waveforms of Full wave rectifier

Operation:

During positive half of the input signal, anode of diode D_1 becomes positive and at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.

During the negative half cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.

It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

Analysis:

Let a sinusoidal voltage V_i be applied to the input of a rectifier. It is given by $V_i=V_m \sin\omega t$
The current i_1 though D_1 and load resistor R_L is given by

$i_1 = I_m \sin\omega t$ for $0 \le \omega t \le \pi$

$i_1 = 0$ for $\pi \le \omega t \le 2\pi$ Where $I_m = \dfrac{V_m}{R_f + R_L}$

Similarly, the current i_2 through diode D_2 and load resistor R_L is given by

$i_2 = 0$ for $0 \le \omega t \le \pi$

$i_2 = I_m \sin\omega t$ for $\pi \le \omega t \le 2\pi$

Therefore, the total current flowing through R_L is the sum of the two currents i_1 and i_2.

i.e., $i_L = i_1 + i_2$.

i) Average (or) DC Output Current (I_{av} or I_{dc}):

The average dc current I_{dc} is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i_1\, d(\omega t) + \frac{1}{2\pi}\int_0^{2\pi} i_2\, d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t\, d(\omega t) + 0 + 0 + \int_{\pi}^{2\pi} I_m \sin\omega t\, d(\omega t)$$

$$= \frac{I_m}{\pi} + \frac{I_m}{\pi}$$

$$= \frac{2I_m}{\pi} = 0.318\ I_m$$

$$\therefore I_{dc} = \frac{2I_m}{\pi}$$

$2 \quad V_m$

Substituting the value of I_m , we get $I_{dc} = \frac{2}{\pi} \frac{V_m}{(R_f + R_L)}$

This is double that of a Half-Wave Rectifier.

ii) Average (or) DC Output Voltage (V_{av} or V_{dc}):

The dc output voltage is given by

$$V_{dc} = I_{dc} \times R_L = \frac{2 I_m R_L}{\pi}$$

$$\Rightarrow V_{dc} = \frac{2}{\pi} \frac{V_m R_L}{R_f + R_L}$$

If $R_L >> R_f$ then $V_{dc} = \frac{2V_m}{\pi}$

iii) R.M.S. Output Current (I_{rms}):

The value of the R.M.S. current is given by

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} i_1^2 \, d(\omega t) + \frac{1}{2\pi}\int_{\pi}^{2\pi} i_2^2 \, d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2 \omega t \, d(\omega t) + \frac{1}{2\pi}\int_{\pi}^{2\pi} I_m^2 \sin^2 \omega t \, d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{2\pi}\int_0^{\pi} \frac{1 - \cos 2\omega t}{2} \, d(\omega t) + \frac{I_m^2}{2\pi}\int_{\pi}^{2\pi} \frac{1 - \cos 2\omega t}{2} \, d(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I^2}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{\omega t}\right]_0^{\pi} + \frac{I^2}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{\omega t}\right]_{\pi}^{2\pi}\right]^{\frac{1}{2}}$$

iv) R.M.S. Output Voltage (V_{rms}):

R.M.S. voltage across the load is given by

$$V_{rms} = I_{rms} \times R_L = \frac{V_m}{\sqrt{2}\left(R_f + R_L\right)} \times R_L$$

$$\Rightarrow V_{rms} = \frac{v_m}{\sqrt{2}\left(1 + \frac{R_f}{R_L}\right)}$$

If $R_L >> R_f$ then $V_{rms} = \frac{V_m}{\sqrt{2}}$

$$= \left[\frac{I_m^2}{4\pi}\left[(\pi - 0) - (0)\right] + \frac{I_m^2}{4\pi}\left[(2\pi - 0) - (\pi - 0)\right]\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi} \times \pi + \frac{I_m^2}{4\pi} \times \pi\right]^{\frac{1}{2}} = \left[2 \times \frac{I_m^2}{4}\right]^{\frac{1}{2}} = \frac{I_m}{\sqrt{2}}$$

$$\therefore I_{rms} = \frac{I_m}{\sqrt{2}} \quad \text{(or)} \quad I_{rms} = \frac{V_m}{\sqrt{2}\left(R_f + R_L\right)}$$

v) Rectifier efficiency(η) :

The rectifier efficiency is defined as the ration of d.c. output power to the a.c. input power i.e.,

$$\eta = P_{dc}/P_{ac}$$

Theoretically the maximum value of rectifier efficiency of a full-wave rectifier is 81.2%

vi) Ripple Factor(γ) :

The ripple factor, γ is given by

$$\therefore \gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \quad \text{(or)} \quad \therefore \gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$\therefore \gamma = \sqrt{\left(\frac{I_m}{\sqrt{2}} \times \frac{\pi}{2\,I_m}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = \mathbf{0.48}$$

$$\Rightarrow \gamma = 0.48$$

vii) Regulation:

The variation of V_{dc} with I_{dc} for a full-wave rectifier is obtained as follows:

$$V_{dc} = I_{dc} \times R_L$$

$$= \frac{2I_m}{\pi} R_L \qquad \because I_{dc} = \frac{2I_m}{\pi}$$

$$= \frac{2V_m R_L}{\pi (R_L + R_f)}$$

$$= \frac{2V_m}{\pi}\left(1 - \frac{R_f}{R_f + R_L}\right) = \frac{2V_m}{\pi} - I_{dc} R_f$$

$$\therefore V_{dc} = \frac{2V_m}{\pi} - I_{dc} R_f$$

The percentage regulation of the Full-wave rectifier is given by

$$\% \text{ Regulation} = \frac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100$$

$$= \frac{\frac{2V_m}{\pi} - \left(\frac{2V_m}{\pi} - I_{dc} R_f\right)}{\frac{2V_m}{\pi} - I_{dc} R_f} \times 100 = \frac{I_{dc} R_f}{I_{dc} R_L} \times 100$$

$$\Rightarrow \% \text{ Regulation} = \frac{R_f}{R_L} \times 100$$

viii) Transformer Utilization Factor (UTF):

The average TUF in full-wave rectifying circuit is determined by considering the primary and secondary winding separately. There are two secondaries here. Each secondary is associated with one diode. This is just similar to secondary of half-wave rectifier. Each secondary has TUF as 0.287.

TUF of primary = P_{dc} / Volt-Amp rating of primary

$$\therefore (TUF)_P = \frac{I_{dc}^2 . R_L}{\frac{I_m}{\sqrt{2}} . \frac{V_m}{\sqrt{2}}} = \frac{\left(\frac{2 I_m}{\pi}\right)^2 . R_L}{\frac{V_m I_m}{2}}$$

$$= \frac{4 I_m^2}{\pi^2} . \frac{2R_L}{I_m^2 (R_f + R_L)} = \frac{8}{\pi^2} \frac{1}{1 + \frac{R_f}{R_L}}$$

If $R_L >> R_f$ then $(TUF)_P = \frac{8}{\pi^2} = 0.812.$

$\therefore (TUF)_{av}$ = P_{dc} / V-A rating of transformer

$$= \frac{(TUF)p + (TUF)s + (TUF)s}{3}$$

$$= \frac{0.812 + 0.287 + 0.287}{3} = 0.693$$

$\therefore (TUF)$ = **0.693**

ix) Peak Inverse Voltage (PIV):

Peak Inverse Voltage is the maximum possible voltage across a diode when it is reverse biased. Consider that diode D_1 is in the forward biased i.e., conducting and diode D_2 is reverse biased i.e., non-conducting. In this case a voltage V_m is developed across the load resistor R_L. Now the voltage across diode D_2 is the sum of the voltages across load resistor R_L and voltage across the lower half of transformer secondary V_m. Hence PIV of diode $D_2 = V_m + V_m = 2V_m$.

Similarly PIV of diode D_1 is $2V_m$.

x) Form factor (F):

The Form Factor F is defined as F = rms value / average value

$$F = \frac{Im/\sqrt{2}}{2\,Im/\pi} = \frac{0.707\,I_m}{0.63\,I_m} = 1.12$$ **F=1.12**

xi) Peak Factor (P):

The peak factor P is defined as

P= Peak Value / rms value $= \frac{I_m}{I_m/\sqrt{2}} = \sqrt{2} = 1.414$ **P = 1.414**

Problems from previous External Question Paper:

4) A Full-Wave rectifier circuit is fed from a transformer having a center-tapped secondary winding. The rms voltage from wither end of secondary to center tap is 30V. if the diode forward resistance is 5J and that of the secondary is 10J for a load of 900J,
Calculate:

- i) Power delivered to load,
- ii) % regulation at full-load,
- iii) Efficiency at full-load and
- iv) TUF of secondary.

Solution: Given V_{rms} = 30V, R_f =5J, Rs=10J, R_L=900J

But $V_{rms} = \frac{V_m}{\sqrt{2}} \Rightarrow V_m = 30 \times \sqrt{2}$ = 42.426 V.

$$I_m = \frac{V_m}{R_f + R_S + R_L} = \frac{30\sqrt{2}}{5 + 10 + 900} = 46.36 \text{ mA.}$$

$$I_{dc} = \frac{2\,Im}{\pi} = \frac{2 \times 46.36}{\pi} = 29.5\text{mA}$$

i) Power delivered to the load $= I_{dc}^2 R_L = \left(29.5 \times 10^{-3}\right)^2 \times 900$ = **0.783W**

ii) % Regulation at full-load = $\frac{V_{no-load} - V_{full-load}}{V_{full-load}} \times 100$

$V_{no-load} = \frac{2V_m}{\pi} = \frac{2 \times 42.426}{\pi}$ = **27.02 V.**

$V_{full-load} = I_{dc} R_L$ = 29.5 x 10^{-3} x 900 = 26.5 V

% Regulation = $\frac{27.02 - 26.5}{26.5} \times 100$ = **1.96 %**

iii) Efficiency of Rectification = $\frac{81.2}{1 + \frac{R_f + R_S}{R_L}} = \frac{81.2}{1 + \frac{15}{900}}$ **= 79.8%**

iv) TUF of secondary = DC power output / secondary ac rating

Transformer secondary rating $= V_{rms} I_{rms} = 30 \times \frac{46.36}{\sqrt{2}} \times 10^{-3}$ W

$P_{dc} = I_{dc}^2 R_L$

$\therefore TUF = \frac{0.783}{30 \times \frac{46.36}{\sqrt{2}} \times 10^{-3}} =$ **0.796**

5) A Full-wave rectifier circuit uses two silicon diodes with a forward resistance of 20J each. A dc voltmeter connected across the load of 1kJ reads 55.4volts. Calculate

i) I_{RMS},
ii) Average voltage across each diode,
iii) Ripple factor, and
iv) Transformer secondary voltage rating.

Solution:

Given R_f =20J, R_L=1kJ, V_{dc} = 55.4V

For a FWR $V_{dc} = \frac{2V_m}{\pi}$ $\therefore V_m = \frac{55.4 \times \pi}{2}$ **= 86.9 V**

$I_m = \frac{V_m}{R_f + R_L}$ **=0.08519A**

i) $I_{rms} = \frac{I_m}{\sqrt{2}}$ = 0.06024A

ii) V= 86.9/2 = 43.45V

iii) Ripple factor

$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$, $I_{dc} = \frac{2I_m}{\pi}$ **=0.05423A** $I_{rms} = \frac{I_m}{\sqrt{2}}$ **=0.06024A**

$\therefore \gamma = 0.48$

iv) Transformer secondary voltage rating: $V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{86.9}{\sqrt{2}}$ = **61.49 Volts.**

6) A 230V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in the Full-wave rectifier having a load of 900J. If the diode resistance and the secondary coil resistance together has a resistance of 100J. Determine:

i) dc voltage across the load,
ii) dc current flowing through the load,
iii) dc power delivered to the load, and
iv) ripple voltage and its frequency.

Solution: Given $V_{p(rms)}$ = 230V

$$\frac{N_2}{N_1} = \frac{2V_{S(rms)}}{V_{P(rms)}} \qquad \Rightarrow \frac{1}{5} = \frac{2V_{S(rms)}}{230}$$

$\Rightarrow V_{S(rms)}$ = 23V

Given R_L =900J, $R_f + R_S$ =100J

$$I_m = \frac{V_{sm}}{R_f + R_S + R_L} = \frac{\sqrt{2}\,V_{s(rms)}}{R_f + R_S + R_L} = \frac{\sqrt{2} \times 23}{900 + 100} = 0.03252 \text{ Amp.}$$

$$\therefore I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 0.03252}{\pi}$$ = **0.0207 Amp.**

i) $V_{DC} = I_{DC} R_L$ = 0.0207 X 100 = **18.6365 Volts.**

ii) I_{DC} = **0.0207 Amp.**

iii) $P_{dc} = I_{dc}^2 R_L$ (or) $V_{DC} I_{DC}$ = **0.3857 Watts.**

iv) PIV = $2V_{sm}$ = 2 X $\sqrt{2}$ X 23 = **65.0538 Volts**

v) Ripple factor = 0.482 = $\frac{V_{r(rms)}}{V_{DC}}$

Therefore, ripple voltage = $V_{r(rms)}$ = 0.482 x 18.6365
= **8.9827 Volts.**

Frequency of ripple = 2f = 2x60 = **120 Hz**

Bridge Rectifier

The full-wave rectifier circuit requires a center tapped transformer where only one half of the total ac voltage of the transformer secondary winding is utilized to convert into dc output. The need of the center tapped transformer in a Full-wave rectifier is eliminated in the bridge rectifier.

The bridge rectifier circuit has four diodes connected to form a bridge. The ac input voltage us applied to diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge. The bridge rectifier circuits and its waveforms are shown in figure.

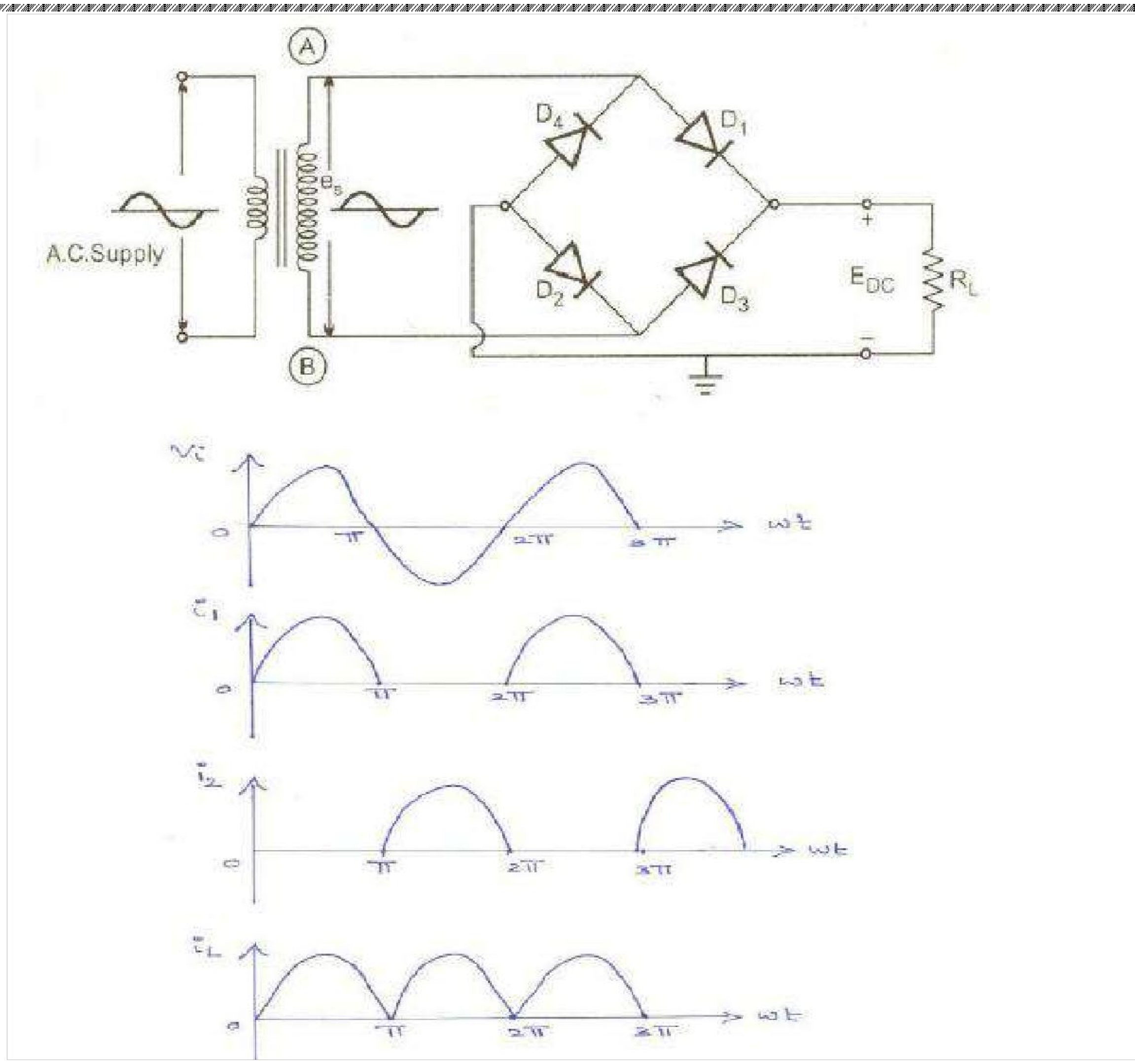


Figure 1.26: Circuit diagram and Input & Output waveforms of Bridge rectifier

Operation:

For the positive half cycle of the input ac voltage diodes D_1 and D_3 conduct, whereas diodes D_2 and D_4 do not conduct. The conducting diodes will be in series through the load resistance R_L, so the load current flows through the R_L.

During the negative half cycle of the input ac voltage diodes D_2 and D_4 conduct, whereas diodes D_1 and D_3 do not conduct.

The conducting diodes D_2 and D_4 will be in series through the load resistance R_L and the current flows through the R_L, in the same direction as in the previous half cycle. Thus a bidirectional wave is converted into a unidirectional wave.

Analysis:

The average values of output voltage and load current, the rms values of voltage and current, the ripple factor and rectifier efficiency are the same as for as center tapped full-wave rectifier.

Hence,

$$V_{dc} = \frac{2V_m}{\pi}$$

$$I_{dc} = \frac{2I_m}{\pi} \qquad I_m = \frac{V_m}{R_f + R_L}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \qquad I_{rms} = \frac{I_m}{\sqrt{2}}$$

Since the each half cycle two diodes conduct simultaneously

$$\gamma = 0.48$$

$$\eta = \frac{81.2}{1 + \frac{2R_f}{R_L}}$$

The transformer utilization factor (TUF) of primary and secondary will be the same as there is always through primary and secondary.

TUF of secondary = P_{dc} / V-A rating of secondary

$$= \frac{I_{dc}^2}{V_{rms} I_{rms}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\frac{V_m}{\sqrt{2}} \frac{I_m}{\sqrt{2}}} = \mathbf{0.812}$$

TUF in case of secondary of primary of FWR is 0.812

$$\therefore (TUF)_{av} = \frac{(TUF)_p + (TUF)_s}{2}$$

$$= \frac{0.812 + 0.812}{2} = \mathbf{0.812}$$

$$\therefore TUF = \mathbf{0.812}$$

The reverse voltage appearing across the reverse biased diodes is $2V_m$, but two diodes are sharing it, therefore the PIV rating of the diodes is V_m.

Advantages of Bridge rectifier circuit:

1) No center-tapped transformer is required.
2) The TUF is considerably high.
3) PIV is reduced across the diode.

Disadvantages of Bridge rectifier circuit:

The only disadvantage of bridge rectifier is the use of four diodes as compared to two diodes for center-tapped FWR. This reduces the output voltage.

Problems:

7. A bridge rectifier uses four identical diodes having forward resistance of 5J and the secondary voltage of $30V_{(rms)}$. Determine the dc output voltage for I_{DC}=200mA and the value of the ripple voltage.

Solution: $V_{s(rms)}$=30V, R_S=5J, R_f=5J, I_{DC}=200mA

Now $I_{DC} = 2\frac{I_m}{\pi}$

$$\therefore I_m = \frac{200 \times 10^{-3} \times \pi}{2} = 0.3415 \text{ Amp.}$$

But $$I_m = \frac{V_{sm}}{R_S + 2R_f + R_L} = \frac{\sqrt{2}\, V_{s(rms)}}{R_S + 2R_f + R_L}$$

$$\Rightarrow 0.3415 = \frac{\sqrt{2} \times 30}{5 + (2 \times 5) + R_L}$$

$\Rightarrow R_L = 120.051\Omega \approx 120\Omega$

$V_{DC} = I_{DC} R_L = 200 \times 10^{-3} \times 120 = 24$Volts

Ripple factor = $\frac{V_{r(rms)}}{V_{dc}}$

For Bridge rectifier, ripple factor = 0.482

$\therefore V_{r(rms)}$ = rms value of ripple voltage

= Vdcx0.482

= 24x0.482

=**11.568 Volts**

8. In a bridge rectifier the transformer is connected to 220V, 60Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diode to be ideal, find:

i) I_{dc}

ii) voltage across the load

iii) PIV assume load resistance to be 1kΩ

Solution: $\frac{N_2}{N_1} = \frac{1}{11}$, $V_{p(rms)} = 220V$, f=60Hz, $R_L = 1k\Omega$

$$\frac{N_2}{N_1} = \frac{V_{S(rms)}}{V_{P(rms)}} \Rightarrow \frac{1}{11} = \frac{V_{S(rms)}}{220} \Rightarrow V_{S(rms)} = \frac{220}{11} = 20V$$

$$V_{sm} = \sqrt{2} V_{s(rms)}$$

i) $$I_m = \frac{V_{sm}}{R_L} = \frac{28.2842}{1 \times 10^{-3}} = 28.2842 \text{ mA}$$

$$\therefore I_{dc} = \frac{2\, I_m}{\pi} = \mathbf{18\ mA}$$

ii) $V_{dc} = I_{dc} R_L = 18 \times 10^{-3} X \times 10^{-3}$ = **18 Volts**

iv) PIV = V_{sm} = **28.2842 Volts**

FILTERS

The output of a half-wave (or) full-wave rectifier circuit is not pure d.c., but it contains fluctuations (or) ripple, which are undesired. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load. Ideally, the output of the filter should be pure d.c. practically, the filter circuit will try to minimize the ripple at the output, as far as possible. Basically, the ripple is ac, i.e., varying with time, while dc is a constant w.r.t. time.

Hence in order to separate dc from ripple, the filter circuit should use components which have widely different impedance for ac and dc. Two such components are inductance and capacitance. Ideally, the inductance acts as a short circuit for dc, but it has large impedance for ac.

Similarly, the capacitor acts as open for dc if the value of capacitance is sufficiently lar enough. Hence, in a filter circuit, the inductance is always connected in series with the load, and tl capacitance is connected in parallel to the load.

Definition of a Filter:

Filter is an electronic circuit composed of a capacitor, inductor (or) combination of both ar connected between the rectifier and the load so as to convert pulsating dc to pure dc.

The different types of filters are:

1) Inductor Filter,
2) Capacitor Filter,
3) LC (or) L-Section Filter, and
4) CLC (or) ∏-section Filter.

Inductor Filter:

Half-Wave rectifier with series Inductor Filter:

The Inductor filter for half-wave rectifier is shown in figure below.

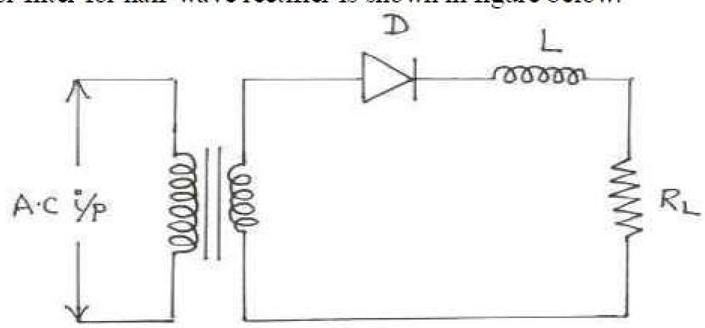


Fig. Series Inductor filter for HWR

In this filter the inductor (choke) is connected in series with the load. The operation of the inductor filter depends upon the property of the inductance to oppose any change of current that may flow through it.

Expression for ripple factor:

For a half-wave rectifier, the output current is given by,

$$i = I_m \left[\frac{1}{\pi} + \frac{1}{2}\sin\omega t - \frac{2}{\pi} \sum_{\substack{K=even \\ K\neq 0}} \frac{\cos\omega t}{(K+1)(K-1)} \right]$$

$$i = \frac{I_m}{\pi} + \frac{I_m}{2}\sin\omega t - \frac{2I_m}{\pi}\left[\frac{\cos 2\omega t}{3} + \frac{\cos 4\omega t}{15} + \ldots\right] \qquad \ldots\ldots\ldots\ldots\ldots (1)$$

Neglecting the higher order terms, we have

$$I_{dc} = \frac{I_m}{\pi} = \frac{V_m}{\pi R_L} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

If I_1 be the rms value of fundamental component of current, then

$$I_{dc} = \frac{I_m}{2\sqrt{2}} = \frac{V_m}{2\sqrt{2}\left(R_L + j\omega L\right)} = \frac{V_m}{2\sqrt{2}\left(R_L^2 + j\omega^2 L^2\right)^{\frac{1}{2}}} \qquad \text{.............(3)}$$

At operating frequency, the reactance offered by inductance 'L' is very large compared to R_L (i.e., $\omega L >> R_L$) and hence R_L can be neglected.

$$\therefore I_1 = \frac{V_m}{2\sqrt{2}\omega L} \qquad \text{.............(4)}$$

If I_2 be rms value of second harmonic,

$$\text{Then } \therefore I_2 = \frac{2I_m}{3\sqrt{2}\pi} = \frac{2V_m}{3\sqrt{2}\pi\left(R_L^2 + 4\omega^2 L^2\right)^{\frac{1}{2}}} = \frac{V_m}{3\sqrt{2}\pi\omega L} \quad \left(\because R_L << \omega L\right) \text{....... (5)}$$

If I_{ac} be the rms value of all current components, then $I_{ac} = \sqrt{I_1^2 + I_2^2}$

$$\text{Now, } \gamma = \frac{V_{ac}}{V_{dc}} = \frac{I_{ac} R_L}{I_{dc} R_L} = \frac{I_{ac}}{I_{dc}}$$

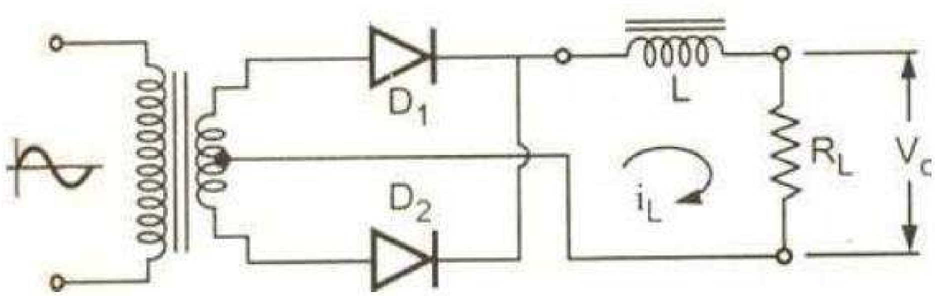
$$= \frac{\sqrt{\left(\frac{V_m}{2\sqrt{2}\omega L}\right)^2 + \left(\frac{V_m}{3\sqrt{2}\pi\omega L}\right)^2}}{\frac{V_m}{\pi R_L}}$$

$$= \frac{\frac{V_m}{\omega L}\sqrt{\frac{1}{8} + \frac{1}{18\pi^2}}}{\frac{V_m}{\pi R_L}} = \frac{\pi R_L}{\omega L}\sqrt{\frac{1}{8} + \frac{1}{18\pi^2}}$$

$$= \frac{1.13 R_L}{\omega L} \qquad \therefore \gamma = \frac{1.13 R_L}{\omega L} \qquad \text{...........(6)}$$

Full-wave rectifier with series inductor filter:

A FWR with series inductor filter is shown in figure.



The inductor offers high impedance to a.c. variations. The inductor blocks the a.c. component and allows only t
he dc component to reach the load.

To analyze the inductor filter for a FWR, the Fourier series can be written as

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left(\frac{1}{3}\cos 2\omega t + \frac{1}{15}\cos 6\omega t + \ldots\ldots\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots(1)$$

The dc component is $\frac{2V_m}{\pi}$

Assuming the third and higher terms contribute little output voltage is

$$V_O = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t \quad \ldots\ldots\ldots\ldots\ldots\ldots(2)$$

For the sake of simplicity, the diode drop and diode resistance are neglected because tl introduce a little error. Thus for dc component, the current $I_m = \frac{V_m}{R_L}$. For ac component, impedance of L and R_L will be in series and is given by,

$$Z = \sqrt{R_L^2 + (2\omega L)^2}$$, frequency of ac component = 2ω

$$= \sqrt{R_L^2 + 4\omega^2 L^2}$$

Thus for ac component $I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}$

The current flowing in a FWR is given by, $i = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi}\cos 2\omega t \ldots\ldots\ldots\ldots\ldots(3)$

Substituting the value of I_m for dc and ac equation (3), we get,

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi\sqrt{R_L^2 + 4\omega^2 L^2}}\cos(2\omega t - \phi) \quad \ldots\ldots\ldots\ldots\ldots(4)$$

Where Φ is the angle by which the load current lags behind the voltage. This is given by

$$\phi = \tan^{-1}\frac{2\omega L}{R_L}$$

Expression for Ripple Factor:

$$\gamma = \frac{I_{r,rms}}{I_{dc}}$$

From equation (4), $I_{dc} = \frac{2V_m}{\pi R_L}$, $I_{r,rms} = \frac{4V_m}{3\pi\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}$

$$\therefore \gamma = \frac{\frac{4V_m}{3\pi\sqrt{2}} \frac{1}{\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}} \qquad \therefore \gamma = \frac{2}{3\sqrt{2}} \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

If $\frac{4\omega^2 L^2}{R_L^2} >> 1$, then $\gamma = \frac{1}{3\sqrt{2}} \frac{R_L}{\omega L} = 0.236 \frac{R_L}{\omega L}$.

$$\therefore \gamma = \frac{R_L}{3\sqrt{2}\omega L} \text{ .... (6)}$$

The expression shows that ripple varies inversely as the magnitude of the inductance, Also, the ripple is smaller for smaller values of R_L i.e., for high currents.

When R_L □□□ the value of □ is given by □ □ $\frac{2}{3\sqrt{2}}$ = 0.471 (close to the value 0.482 of rectifier). Thus the inductor filter should be used when R_L is consistently small.

Problems:

9. A full-wave rectifier with a load resistance of 15kJ uses an inductor filter of 15H. The peak value of the applied voltage is 250V and the frequency is 50 cycles/second. Calculate the dc load current, ripple factor and dc output voltage.

Solution: The rectified output voltage across load resistance R_L up to second harmonic is

$$V_0 = \frac{2V_m}{\pi} - \frac{2V_m}{\pi}\cos\omega t$$

Therefore, DC component of output voltage is given by $V_{dc} = \frac{2V_m}{\pi}$

$$\therefore I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L}$$

$$= \frac{2 \times 250}{\pi \times 15 \times 10^{-3}} = 10.6 \times 10^{-3} \text{ A} = 10.6 \text{ mA}$$

$V_{dc} = I_{dc} R_L = (2.12\times10^{-3})(15\times10^{3}) = 31.8$ V.

Peak value of ripple voltage = $\frac{4V_m}{3\pi}$

$$\therefore V_{ac} = \frac{1}{\sqrt{2}} \frac{4V_m}{3\pi}$$

$$\text{Now } I_{ac} = \frac{\frac{1}{\sqrt{2}} \frac{4V_m}{3\pi}}{\sqrt{R_L^2 + (2\omega L)^2}} = \frac{2\sqrt{2}V_m}{3\pi\sqrt{R_L^2 + (2\omega L)^2}}$$

$$= \frac{2 \times 1.414 \times 250}{3 \times 3.14\sqrt{(15 \times 10^3) + (4 \times 3.14 \times 50 \times 15)^2}}$$

$= 4.24\times10^{-3}$ A = **4.24 mA**

So, ripple factor, $\gamma = \frac{I_{ac}}{I_{dc}} = \frac{4.24mA}{10.6mA} =$ **0.4**

Capacitor Filter:

Half-wave rectifier wit capacitor filter:

The half-wave rectifier with capacitor input filter is shown in figure below:

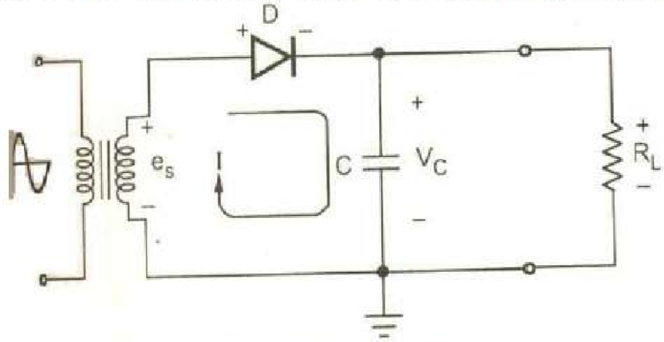


Fig. HWR with capacitor filter.

The filter uses a single capacitor connected in parallel with the load R_L. In order to minimize the ripple in the output, the capacitor C used in the filter circuit is quite large of the order of tens of microfarads.

The operation of the capacitor filter depends upon the fact that the capacitor stores energy during the conduction period and delivers this energy to the load during non-conduction period.

Operation:

During, the positive quarter cycle of the ac input signal, the diode D is forward biased and hence it conducts. This quickly charges the capacitor C to peak value of input voltage V_m. Practically the capacitor charge (V_m-$V\gamma$) due to diode forward voltage drop.

When the input starts decreasing below its peak value, the capacitor remains charged at V_m and the ideal diode gets reverse biased. This is because the capacitor voltage which is cathode voltage of diode becomes more positive than anode.

Therefore, during the entire negative half cycle and some part of the next positive half cycle, capacitor discharges through R_L. The discharging of capacitor is decided by R_LC, time constant which is very large and hence the capacitor discharge very little from V_m.

In the next positive half cycle, when the input signal becomes more than the capacitor voltage, he diode becomes forward biased and charges the capacitor C back to V_m. The output waveform is shown in figure below:

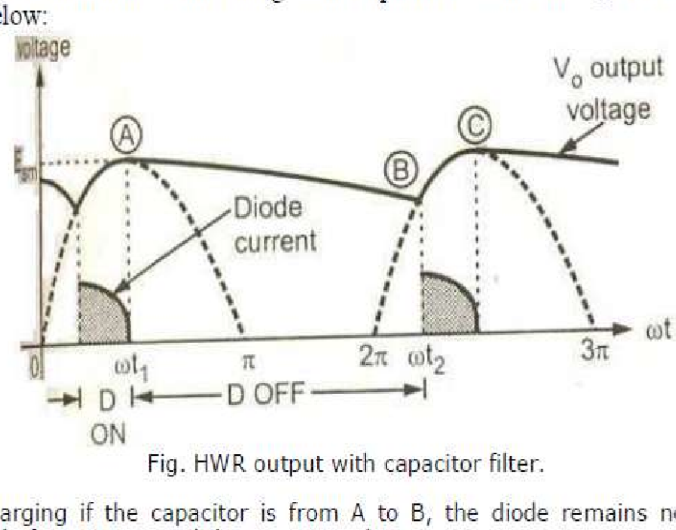
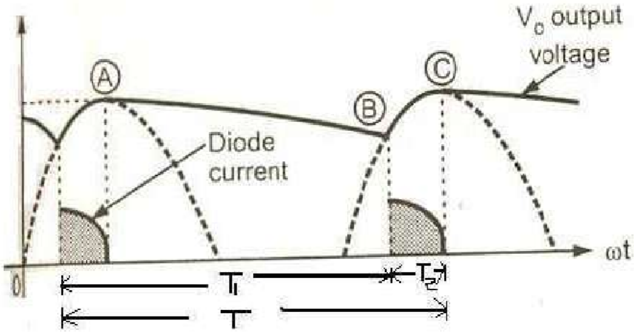


Fig. HWR output with capacitor filter.

The discharging if the capacitor is from A to B, the diode remains non-conducting. The diode conducts only from B to C and the capacitor charges.

Expression for Ripple factor:



Let, T = time period of the ac input voltage

T_1 = time for which the diode is non conducting.

T_2 = time for which diode is conducting.

Let V_r be the peak to peak value of the ripple voltage which is assumed to be triangular waveform. It is known mathematically that the rms value of such a triangular waveform is

$$V_{rms} = \frac{V_r}{2\sqrt{3}}$$

During the time interval T_1, the capacitor C is discharging through the load resistance R_L. Therefore the charge lost is **$Q = C\ V_r$**

But, $i = \frac{dQ}{dt}$ $\quad \therefore Q = \int_0^{T_1} i\,dt = I_{dc} \cdot T_1$

As integration gives average (or) dc value,

Hence $I_{dc} \cdot T_1 = C \cdot V_r$

$$\therefore V_r = \frac{I_{dc} T_1}{C}$$

But $T_1 + T_2 = T$ Normally, $T_1 >> T_2$,

$$\therefore T_1 + T_2 \approx T_1 \Rightarrow T_1 = T$$

$$\therefore V_r = \frac{I_{dc} \cdot T}{C} = \frac{I_{dc}}{f \cdot C} \qquad \therefore T = \frac{1}{f}$$

But $I_{dc} = \frac{V_{dc}}{R_L}$, $\quad V_{dc} = V_m - \frac{V_r}{2}$, $= V_m - \frac{I_{dc}}{2fc}$

$$\therefore V_r = \frac{V_{dc}}{fCR_L}$$

Ripple factor, $\gamma = \frac{V_{rms}}{V_{dc}}$ $\quad \Rightarrow \gamma = \frac{V_r}{2\sqrt{3} \cdot V_{dc}} = \frac{V_{dc}}{2\sqrt{3} fCR_L \cdot V_{dc}}$

$$\gamma \Rightarrow \frac{1}{2\sqrt{3}\, fCR_L}$$

The product of CR_L is the time constant of the filter circuit.

Surge current in Half-wave rectifier using capacitor filter:

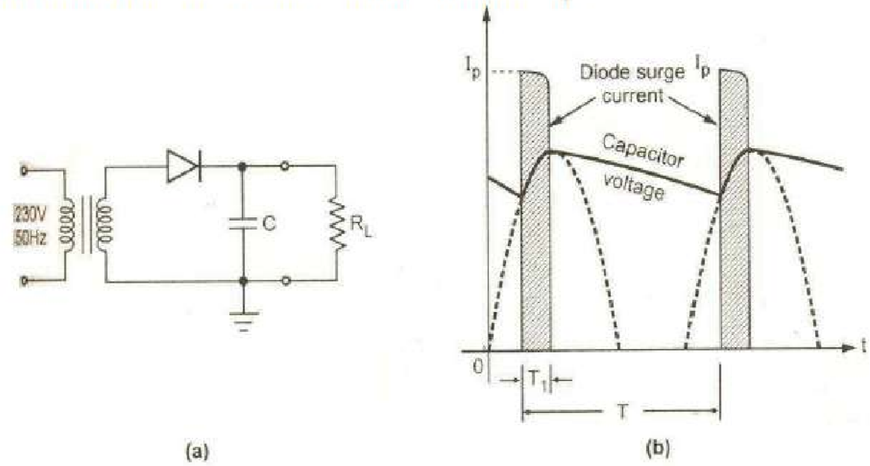


Fig. Surge current in HWR using capacitor filter

In half-wave rectifier, the diode is forward biased only for short period of time and conducts only during this time interval to charge the filter capacitance. The instant at which the diode gets forward biased, the capacitor instantaneously acts as short circuit and a surge current flow through a diode.

When the diode is non-conducting, the capacitor discharges through load resistance R_L. Thus total amount of charge that flows through conducting diode (or) diodes to recharge the capacitor must be equal to the amount of charge lost during the period when the diode (or) diodes are non-conducting and capacitor is discharging through load resistance R_L.

It can be seen that conduction period T_1 is very small compared to time period T, for the diode. Let, I_{dc} = average dc current

$I_{p(surge)}$ = peak value of the surge current.

Assume the current pulse to be rectangular assuming peak surge current flows for the entire conduction period of diode which is T_1.

Then Q (discharge) = Q (charge)

$$\therefore I_{dc} T = I_{P(surge)} T_1 \qquad \therefore I_{P(surge)} = I_{dc} \frac{T}{T_1}$$

As $T_1 << T$, it can be observed that $I_{p(surge)}$ can be many times larger than the average dc current supplied to the load.

Problem from previous External examinations:

10. A HWR circuit has filter capacitor of 1200μF and is connected to a load of 400J. The rectifier is connected to a 50Hz, 120V rms source. It takes 2msec for the capacitor to recharge during each cycle. Calculate the minimum value of the repetitive surge current for which the diode should be rated.

Solution:

Given C=1200μF, R_L=400J, f=50Hz, V_{rms}=120V

Conduction period of the diode, T_1=1ms

$$V_{sm} = \sqrt{2} \times V_{S(rms)} = \sqrt{2} \times 120 \text{ V}$$

$$V_{dc} = V_{sm} - \frac{I_{dc}}{2fC}$$

$$\Rightarrow V_{dc} = V_{sm} - \frac{V_{dc}}{2fCR_L}$$

$$\Rightarrow V_{dc} = \frac{V_{sm}}{1 + \frac{1}{2fCR_L}}$$

$$= \frac{120\sqrt{2}}{1 + \frac{1}{2 \times 50 \times 1200 \times 10^{-6} \times 400}} = 3.46 \text{ V}$$

$$\therefore I_{dc} = \frac{V_{dc}}{R_L} = \frac{3.46}{400} = 8.658\text{mA}$$

Now $I_{dc} T = I_{p(surge)} t_1$

$$I_{P(surge)} = I_{dc} \frac{T}{t_1} = 8.658\text{mA} \times \frac{1}{50 \times 10^{-3}}$$

$$\therefore I_{P(surge)} = 0.17316 \text{ A}$$

Full-wave rectifier with capacitor filter:

The full-wave rectifier with capacitor filter is shown in the figure below:

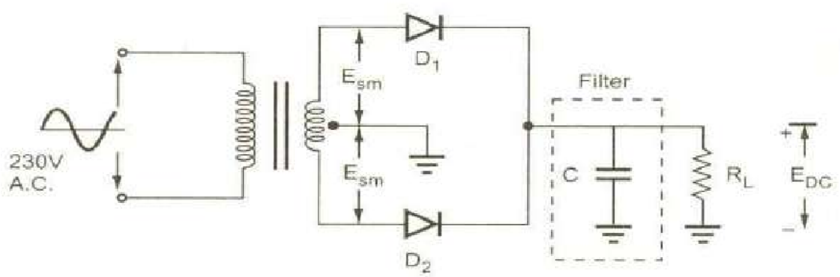


Fig. Full-wave rectifier with capacitor filter

Operation:

During the positive quarter cycle of the ac input signal, the diode D_1 is forward biased, the capacitor C gets charges through forward bias diode D_1 to the peak value of input voltage V_m.

In the next quarter cycle from $\frac{\pi}{2}$ to π the capacitor starts discharging through R_L, because once the capacitor gets charges to V_m, the diode D_1 gets reverse biased and stops conducting, so during the period from $\frac{\pi}{2}$ to π the capacitor C supplies the load current.

In the next quarter half cycle, that is, π to $\frac{3\pi}{2}$ of the rectified output voltage, if the input voltage exceeds the capacitor voltage, making D_2 forward biased, this charges the capacitor back to V_m.

In the next quarter half cycle, that is, from $\frac{3\pi}{2}$ to 2π, the diode gets reverse biased and the capacitor supplies the load current.

In FWR, as the time required by the capacitor to charge is very small and it discharges very little due to large time constant, hence ripple in the output gets reduced considerably. The output waveform is shown in figure below:

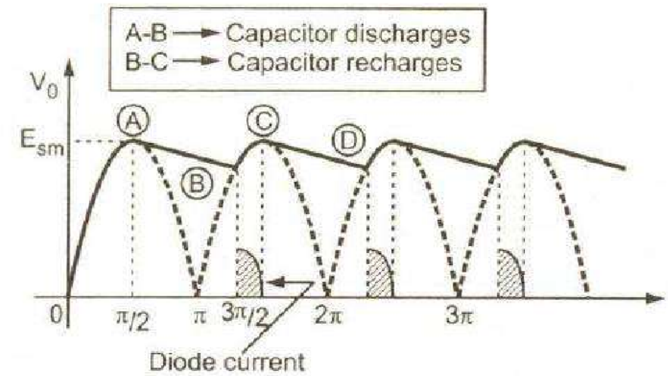
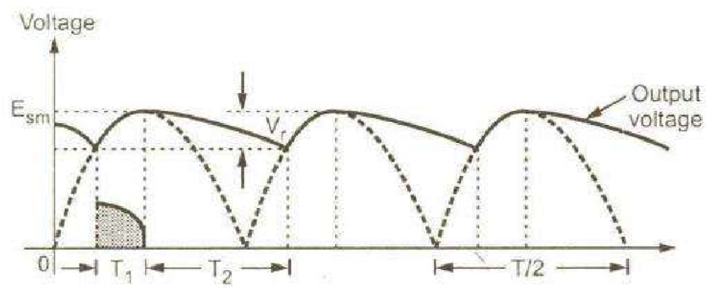


Fig. FWR output with capacitor filter.

Expression for Ripple factor:



Let, T = time period of the ac input voltage

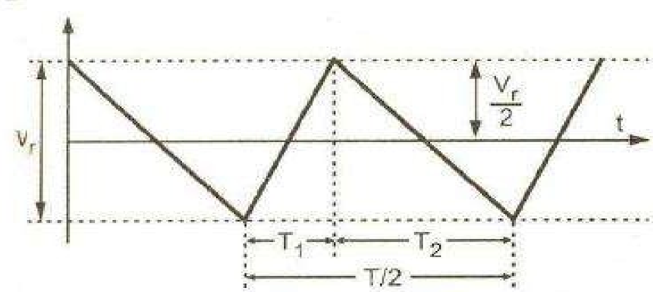
$\frac{T}{2}$ = half of the time period

T_1 = time for which diode is conducting

T_2 = time for which diode is non-conducting

During time T_1, capacitor gets charged and this process is quick. During time T_2, capacitor gets discharged through R_L. As time constant R_LC is very large, discharging process is very slow and hence $T_2 >> T_1$.

Let V_r be the peak to peak value of ripple voltage, which is assumed to be triangular as shown in the figure below:



It is known mathematically that the rms value of such a triangular waveform is,

$$V_{rms} = \frac{V_r}{2\sqrt{3}}$$

During the time interval T_2, the capacitor C is discharging through the load resistance R_L.

The charge lost is, $Q = CV_r$ But $i = \frac{dQ}{dt}$

$$\therefore Q = \int_0^{T_2} i\,dt = I_{DC} T_2$$

As integration gives average (or) dc value, hence $I_{dc} . T_2 = C . V_r$

$$\therefore V_r = \frac{I_{dc} T_2}{C} \qquad \text{But } T_1 + T_2 = \frac{T}{2}$$

Normally, $T_2 >> T_1$,

$$\therefore T_1 + T_2 \approx T_1 = \frac{T}{2} \quad \text{where } T = \frac{1}{f}$$

$$\therefore V_r = \frac{I_{DC}}{C}\frac{T}{2} = \frac{I_{DC} \times T}{2C} = \frac{I_{DC}}{2fC}$$

But $I_{DC} = \frac{V_{DC}}{R_L}$, $\therefore V_r = \frac{V_{DC}}{2fCR_L}$ = peak to peak ripple voltage

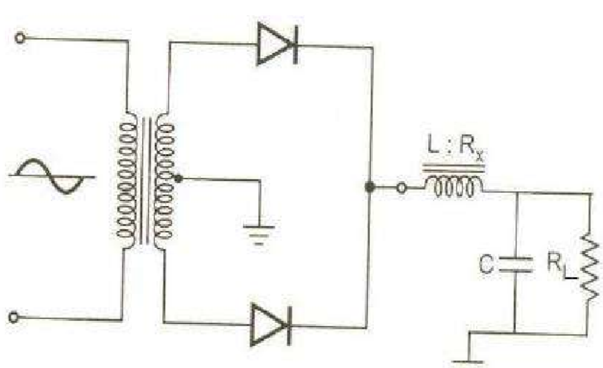
$$\text{Ripple factor,} = \frac{V_{rms}}{V_{dc}} = \frac{\frac{V_{dc}}{2fCRL}}{2\sqrt{3}} \times \frac{1}{V_{dc}} \qquad \therefore V_{rms} = \frac{V_r}{2\sqrt{3}}$$

$$\therefore \text{Ripple factor} = \frac{1}{4\sqrt{3} fCR_L}$$

L-Section Filter (or) LC Filter:

The series inductor filter and shunt capacitor filter are not much efficient to provide low ripple at all loads. The capacitor filter has low ripple at heavy loads while inductor filter at small loads. A combination of these two filters may be selected to make the ripple independent of load resistance. The resulting filter is called L-Section filter (or) LC filter (or) Choke input filter. This

name is due to the fact that the inductor and capacitor are connected as an inverted L. A full-wave rectifier with choke input filter is shown in figure below:



The action of choke input filter is like a low pass filter. The capacitor shunting the load bypasses the harmonic currents because it offers very low reactance to a.c. ripple current while it appears as an open circuit to dc current.

On the other hand the inductor offers high impedance to the harmonic terms. In this way, most of the ripple voltage is eliminated from the load voltage.

Regulation:

The output voltage of the rectifier is given by, $v = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t$

The dc voltage at no load condition is $V_{dc} = \frac{2V_m}{\pi}$

The dc voltage on load is $V_{dc} = \frac{2V_m}{\pi} - I_{dc} R$

Where $R = R_f + R_C + R_S$

R_f, R_C, R_S are resistances of diode, choke an secondary winding.

Ripple Factor:

The main aim of the filter is to suppress the harmonic components. So the reactance of the choke must be large as compared with the combined parallel impedance of capacitor and resistor.

The parallel impedance of capacitor and resistor can be made small by making the reactance of the capacitor much smaller than the resistance of the load. Now the ripple current which has passed through L will not develop much ripple voltage across R_L because the reactance of C at the ripple frequency is very small as compared with R_L.

Thus for LC filter, $X_L >> X_C$ at $2\omega = 4\Pi f$ and $R_L >> X_C$

Under these conditions, the a.c. current through L is determined primarily by $X_L = 2\omega L$ (the reactance of the inductor at second harmonic frequency). The rms value of the ripple current is

$$I_{r(rms)} = \frac{4V_m}{3\pi\sqrt{2}} \frac{1}{X_L} = \frac{2}{3\sqrt{2}X_L}\frac{2V_m}{\pi} = \frac{\sqrt{2}}{3X_L}(V_{dc})$$

Always it was stated that X_C is small as compared with R_L, but it is not zero. The a.c. voltage across the load (the ripple voltage) is the voltage across the capacitor.

Hence $V_{r(rms)} = I_{r(rms)} \times X_C$

$$= \frac{\sqrt{2}}{3X_L} V_{dc} \quad X_C$$

We know that ripple factor γ is given by

$$\gamma = \frac{V_{r(rms)}}{V_{dc}} = \frac{\sqrt{2}X_C}{3X_L}$$

But $X_C = \frac{1}{2\omega C}$ and $X_L = 2\omega L$

$$\therefore \gamma = \frac{\sqrt{2}}{3(2\omega L)} \times \frac{1}{2\omega C} = \frac{1}{6\sqrt{2}\omega^2 LC}$$

$$\therefore \gamma = \frac{1}{6\sqrt{2}\omega^2 LC}$$

This shows that ω is independent of R_L.

Multiple L-Section filters:

The number of L-sections i.e., LC circuits can be connected one after another to obtain multiple L-section filter. It gives excellent filtering and smooth dc output voltage. The figure below shows multiple L-section filter.

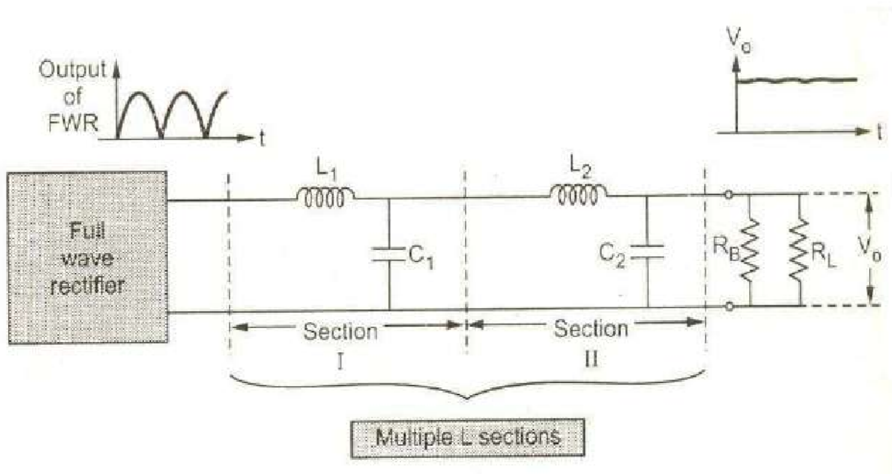


Fig. Multiple L-sections.

For two section LC filter, the ripple factor is given by

$$\Rightarrow \gamma = \frac{\sqrt{2}}{3}\cdot\frac{X_{C1}}{X_{L1}}\cdot\frac{X_{C}}{X_{L2}}$$

CLC Filter (or) Π – section Filter:

This is capacitor input filter followed by a L-section filter. The ripple rejection capability of a Π-section filter is very good. The full-wave rectifier with Π-section filter is shown in the figure.

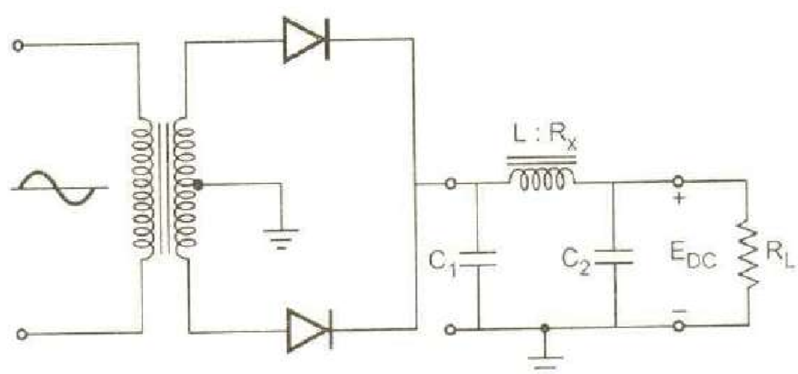


Fig. Π-section Filter.

It consists of an inductance L with a dc winding resistance as R_C and two capacitors C_1 and C_2. The filter circuit is fed from fill wave rectifier. Generally two capacitors are selected equal.

The rectifier output is given to the capacitor c_1. This capacitor offers very low reactance to the ac component but blocks dc component. Hence capacitor C_1 bypasses most of the ac component. The dc component then reaches to the choke L. The choke L offers very high reactance to dc. So it blocks ac component and does not allow it to reach to load while it allows dc component to pass through it. The capacitor C_2 now allows to pass remaining ac component and almost pure dc component reaches to the load. The circuit looks like a Π, hence called Π-Filter.

Ripple Factor:

The Fourier analysis of a triangular wave is given by

$$v = V_{dc} - \frac{V}{\pi}\left(\sin \omega t - \frac{\sin 4\omega t}{2} + \frac{\sin 6\omega t}{3} ....\right) \quad ....(1)$$

In case of full wave rectifier with capacitor filter, we have proved that

$$V_\gamma = \frac{I_{dc}}{2fC} = \frac{I_{dc}}{2fC_1} \quad \left(\therefore C = C_1 \, here\right) \quad ....(2)$$

The rms second harmonic voltage is

$$V_{r(rms)} = \frac{V_r}{\sqrt{2}} \quad ....(3)$$

Substituting the value of V_r from equation (2) in equation (3), we get

$$V_{r(rms)} = \frac{I_{dc}}{2\pi f C_1 \sqrt{2}} = \sqrt{2}\, I_{dc} \, XC_1 \quad ....(4)$$

Where $XC_1 = \frac{1}{2\omega C_1} = \frac{1}{4\pi f C_1}$ = reactance of C_1 at second harmonic frequency.

The voltage $V_{r(rms)}$ is impressed on L-section.

Now, the ripple voltage $V'_{r(rms)}$ can be obtained by multiplying $V_{r(rms)}$ by $\frac{XC_2}{X_L}$ i.e.,

$$\left(V'_r\right)_{rms} = \left(V_r\right)_{rms} \times \frac{XC_1}{X_L}$$

(or) $$\left(V'_r\right)_{rms} = \sqrt{2}\, I_{dc} \, XC_1 . \frac{XC_2}{X_L} \quad ....(5)$$

$$\therefore \gamma = \frac{\left(V'_r\right)_{rms}}{V_{dc}} = \frac{\sqrt{2}\, I_{dc} \, XC_1 . \frac{XC_2}{XL}}{V_{dc}}$$

$$\Rightarrow \gamma = \frac{\sqrt{2}. XC_1 . XC_2}{R_L X_L} \qquad \because \frac{I_{dc}}{V_{dc}} = \frac{1}{R_L}$$

$$\therefore \gamma = \frac{\sqrt{2}. XC_1 . XC_2}{R_L X_L}$$

Here all reactances are calculated at second harmonic frequency. Substituting the values, we get

$$\gamma = \frac{\sqrt{2}}{8\omega^3 C_1 C_2 L R_L}$$

At f= 50Hz, $\gamma = \frac{5700}{LC_1C_2R_L}$

Where C_1 and C_2 are in μF, L in henrys and R_L in ohms.

Multiple Π-Section Filter:

To obtain almost pure dc to the load, more Π-sections may be used one after another. Such a filter using more than one Π-section is called multiple Π-section filter. The figure shows multiple Π-section filters.

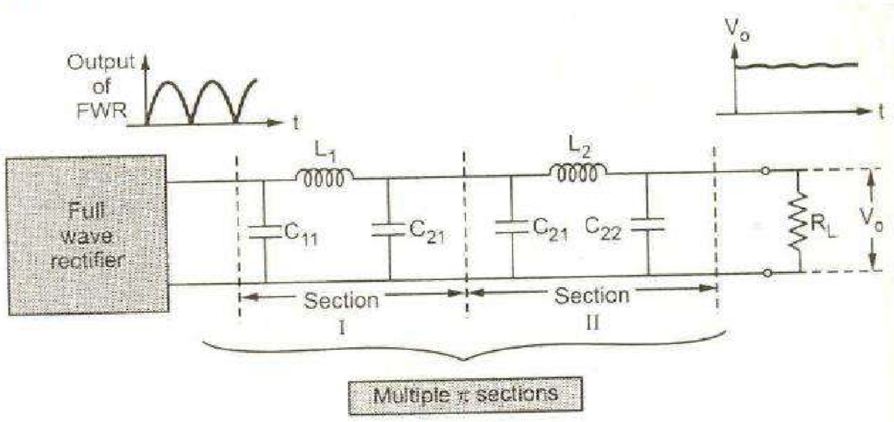


Fig. Multiple Π-section Filter.

The ripple factor of two section Π-filter is given by $\gamma = \sqrt{2}\,\dfrac{X_{C11}}{R_L}\cdot\dfrac{X_{C12}}{X_1}\cdot\dfrac{X_{C22}}{X_2}$

Problems:

14. Design a CLC (or) Π-section filter for V_{dc}=10V, I_L=200mA and γ=2%

Solution:

$$R_L = \frac{V_{dc}}{I_L} = \frac{10}{200\times10^{-3}} = 50J$$

$$\gamma = \frac{5700}{LC_1C_2R_L} \qquad \Rightarrow 0.02 = \frac{5700}{LC_1C_2R_L} = \frac{114}{LC_1C_2}$$

If we assume L=10H and C_1=C_2=C, we have

$$\Rightarrow 0.02 = \frac{114}{LC^2} = \frac{11.4}{C^2}$$

$C^2 = 750 \Rightarrow \sqrt{570}$ = **24μF**

UNIT-II
SPECIAL PURPOSE ELECTONIC DEVICES

ZENER DIODE:

When the reverse voltage reaches breakdown voltage in normal PN junction diode, the current through the junction and the power dissipated at the junction will be high. Such an operation is destructive and the diode gets damaged. Whereas diodes can be designed with adequate power dissipation capabilities to operate in a break down
region. One such a diode is known as Zener diode.

Zener diode is heavily doped than the ordinary diode. Due to this the depletion layer will be very thin and for small applied reverse voltage(V_R) there will be sharp increase in current.

From the V-I characteristics of the Zener diode, shown in figure. It is found that the operation of Zener diode is same as that of ordinary PN diode.
Under forward-biased condition.Whereas under reverse-biased condition, breakdown of the junction occurs. The breakdown voltage depends upon the amount of doping. If the diode is heavily doped, depletion layer will be thin and consequently, breakdown occurs at lower reverse voltage and further, the breakdown voltage is sharp. Whereas a lightly doped diode has a higher breakdown voltage. Thus breakdown voltage can be selected with the amount of doping.

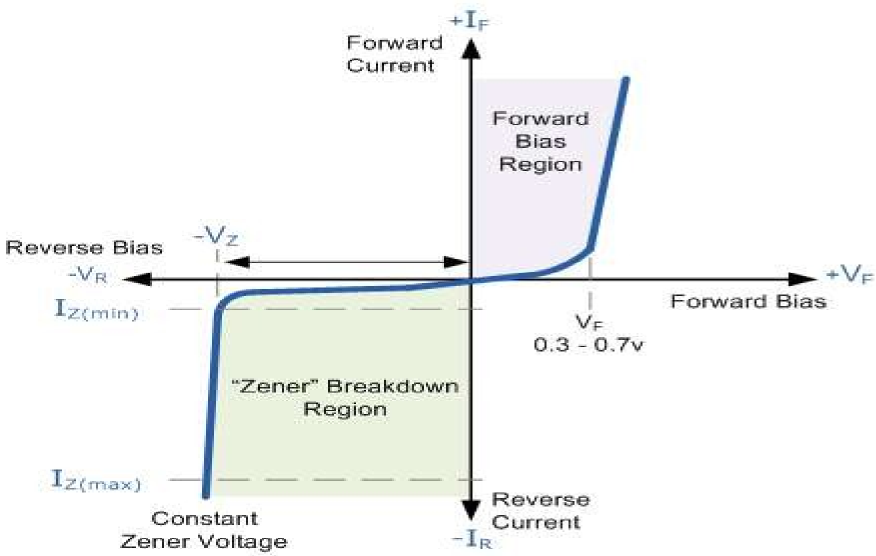


Figure 2.1: V-I Characteristics of a Zener diode

Note:

A heavily doped diode has a low Zener breakdown voltage, while a lightly doped diode has a high Zener breakdown voltage.

ZENER BREAKDOWN MECHANISM:

The sharp increasing current under breakdown conditions is due to the following two mechanisms.
(1) Avalanche breakdown
(2) Zener breakdown

The breakdown in the Zener diode at the voltage V_z may be due to any of the following mechanisms.

1. Avalanche breakdown

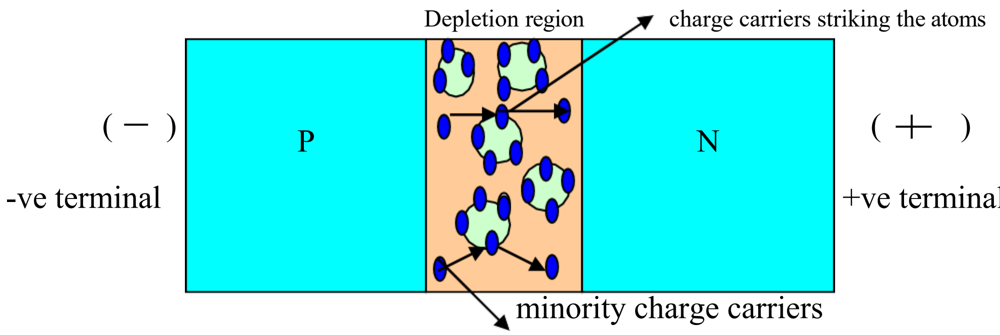


Figure 2.2: Avalanche breakdown in Zener diode

- We know that when the diode is reverse biased a small reverse saturation current I_0 flows across the junction because of the minority cariers in the depletion region.

- The velocity of the minority charge carriers is directly proportional to the applied voltage. Hence when the reverse bias voltage is increased, the velocity of minority charge carriers will also increase and consequently their energy content will also increase.

- When these high energy charge carriers strikes the atom within the depletion region they cause other charge carriers to break away from their atoms and join the flow of current across the junction as shown above. The additional charge carriers generated in this way strikes other atoms and generate new carriers by making them to break away from their atoms.

- This cumulative process is referred to as avalanche multiplication which results in the flow of large reverse current and this breakdown of the diode is called avalanche breakdown.

2. Zener breakdown

We have electric field strength = Reverse voltage/ Depletion region

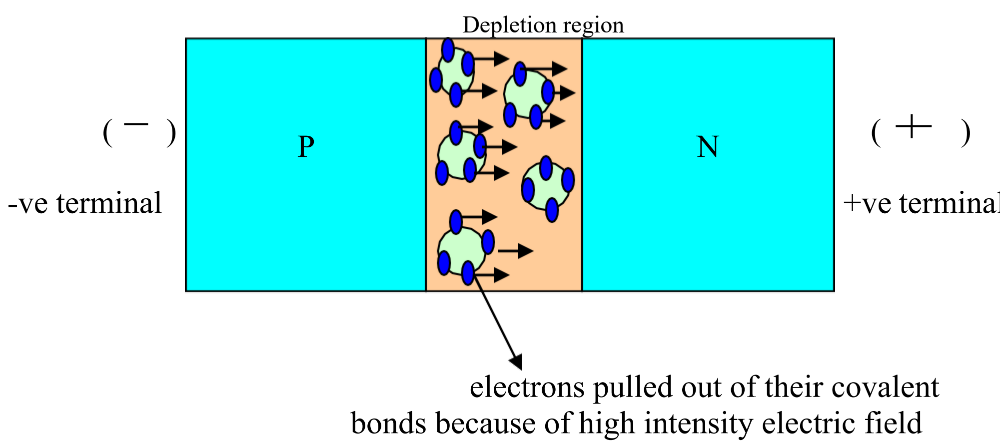


Figure 2.3: Zener breakdown in Zener diode

From the above relation we see that the reverse voltage is directly proportional to the electric field hence, a small increase in reverse voltage produces a very high intensity electric field with ina narrow Depletion region.

Therefore when the reverse voltage to a diode is increased, under the influence of high intensity electric filed large numbr of electrons within the depletion region break the covalent bonds with their atoms as shown above and thus a large reverse current flows through the diode. This breakdown is referred to as Zener breakdown.

Zener Diode as Voltage Regulator:

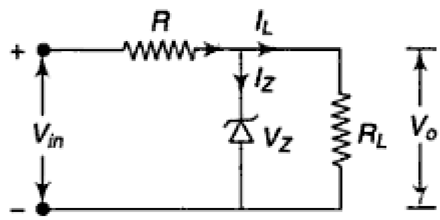


Figure 2.4: Zener diode as voltage regulator

From the Zener Characteristics shown, under reverse bias condition, the voltage across the diode remains constant although the current through the diode increases as shown. Thus the voltage across the zener diode serves as a reference voltage. Hence the diode can be used as a voltage regulator.
It is required to provide constant voltage across load resistance R_L , whereas the input voltage may be varying over a range. As shown, zener diode is reverse biased and as long as the input voltage does not fall below v_z (zener breakdown voltage), the voltage across the diode will be constant and hence the load voltage will also be constant.

Light Emitting Diode:

Light Emitting Diodes or **LED´s**, are among the most widely used of all the different types of semiconductor diodes available today and are commonly used in TV's and colour displays.
They are the most visible type of diode, that emit a fairly narrow bandwidth of either visible light at different coloured wavelengths, invisible infra-red light for remote controls or laser type light when a forward current is passed through them.

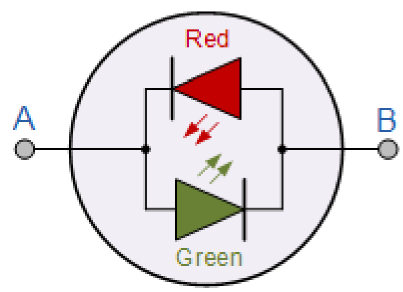


Figure 2.4: The Light Emitting Diode

The "**Light Emitting Diode**" or **LED** as it is more commonly called, is basically just a specialised type of diode as they have very similar electrical characteristics to a PN junction diode. This means that an LED will pass current in its forward direction but block the flow of current in the reverse direction.
Related Products: LEDs and LED Lighting | Optical Lenses
Light emitting diodes are made from a very thin layer of fairly heavily doped semiconductor material and depending on the semiconductor material used and the amount of doping, when forward biased an LED will emit a coloured light at a particular spectral wavelength.
When the diode is forward biased, electrons from the semiconductors conduction band recombine with holes from the valence band releasing sufficient energy to produce photons which emit a monochromatic (single colour) of light. Because of this thin layer a reasonable number of these photons can leave the junction and radiate away producing a coloured light output.

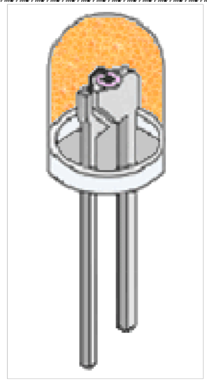


Figure 2.5: LED Construction

Then we can say that when operated in a forward biased direction **Light Emitting Diodes** are semiconductor devices that convert electrical energy into light energy.

The construction of a Light Emitting Diode is very different from that of a normal signal diode. The PN junction of an LED is surrounded by a transparent, hard plastic epoxy resin hemispherical shaped shell or body which protects the LED from both vibration and shock.

Surprisingly, an LED junction does not actually emit that much light so the epoxy resin body is constructed in such a way that the photons of light emitted by the junction are reflected away from the surrounding substrate base to which the diode is attached and are focused upwards through the domed top of the LED, which itself acts like a lens concentrating the amount of light. This is why the emitted light appears to be brightest at the top of the LED.

However, not all LEDs are made with a hemispherical shaped dome for their epoxy shell. Some indication LEDs have a rectangular or cylindrical shaped construction that has a flat surface on top or their body is shaped into a bar or arrow. Generally, all LED's are manufactured with two legs protruding from the bottom of the body.

Also, nearly all modern light emitting diodes have their cathode, (–) terminal identified by either a notch or flat spot on the body or by the cathode lead being shorter than the other as the anode (+) lead is longer than the cathode (k).

Unlike normal incandescent lamps and bulbs which generate large amounts of heat when illuminated, the light emitting diode produces a "cold" generation of light which leads to high efficiencies than the normal "light bulb" because most of the generated energy radiates away within the visible spectrum. Because LEDs are solid-state devices, they can be extremely small and durable and provide much longer lamp life than normal light sources.

Light Emitting Diode Colours:

So how does a light emitting diode get its colour. Unlike normal signal diodes which are made for detection or power rectification, and which are made from either Germanium or Silicon semiconductor materials, **Light Emitting Diodes** are made from exotic semiconductor compounds such as Gallium Arsenide (GaAs), Gallium Phosphide (GaP), Gallium Arsenide Phosphide (GaAsP), Silicon Carbide (SiC) or Gallium Indium Nitride (GaInN) all mixed together at different ratios to produce a distinct wavelength of colour.

Different LED compounds emit light in specific regions of the visible light spectrum and therefore produce different intensity levels. The exact choice of the semiconductor material used will determine the overall wavelength of the photon light emissions and therefore the resulting colour of the light emitted.

Thus, the actual colour of a light emitting diode is determined by the wavelength of the light emitted, which in turn is determined by the actual semiconductor compound used in forming the PN junction during manufacture.

Therefore the colour of the light emitted by an LED is NOT determined by the colouring of the LED's plastic body although these are slightly coloured to both enhance the light output and to indicate its colour when its not being illuminated by an electrical supply.

Light emitting diodes are available in a wide range of colours with the most common being RED, AMBER, YELLOW and GREEN and are thus widely used as visual indicators and as moving light displays.

Recently developed blue and white coloured LEDs are also available but these tend to be much more expensive than the normal standard colours due to the production costs of mixing together two or more complementary colours at an exact ratio within the semiconductor compound and also by injecting nitrogen atoms into the crystal structure during the doping process.

Light Emitting Diode Colours:

From the table shown below we can see that the main P-type dopant used in the manufacture of **Light Emitting Diodes** is Gallium (Ga, atomic number 31) and that the main N-type dopant used is Arsenic (As, atomic number 33) giving the resulting compound of Gallium Arsenide (GaAs) crystalline structure.

The problem with using Gallium Arsenide on its own as the semiconductor compound is that it radiates large amounts of low brightness infra-red radiation (850nm-940nm approx.) from its junction when a forward current is flowing through it.

The amount of infra-red light it produces is okay for television remote controls but not very useful if we want to use the LED as an indicating light. But by adding Phosphorus (P, atomic number 15), as a third dopant the overall wavelength of the emitted radiation is reduced to below 680nm giving visible red light to the human eye. Further refinements in the doping process of the PN junction have resulted in a range of colours spanning the spectrum of visible light as we have seen above as well as infra-red and ultra-violet wavelengths.

Typical LED Characteristics			
Semiconductor Material	Wavelength	Colour	V_F @ 20mA
GaAs	850-940nm	Infra-Red	1.2v
GaAsP	630-660nm	Red	1.8v
GaAsP	605-620nm	Amber	2.0v
GaAsP:N	585-595nm	Yellow	2.2v
AlGaP	550-570nm	Green	3.5v
SiC	430-505nm	Blue	3.6v
GaInN	450nm	White	4.0v

By mixing together a variety of semiconductor, metal and gas compounds the following list of LEDs can be produced.

Liquid crystal display:

We always use devices made up of Liquid Crystal Displays (LCDs) like computers, digital watches and also DVD and CD players. They have become very common and have taken a giant leap in the screen industry by clearly replacing the use of Cathode Ray Tubes (CRT). CRT draws more power than LCD and are also bigger and heavier. All of us have seen an LCD, but no one knows the exact working of it. Let us take a look at the working of an LCD.

Figure 2.6: LCD

The article below is developed as two sections:-

1. Basics of LCD Displays 2. Working Principle of LCD

Note:- If you are looking for a note on technical specifications of LCD Displays for Interfacing it with micro controllers:- here we have a great article on the same:- A Note on Character LCD Display.If you want to know about the invention history of LCD go through the article:- Invention History of Liquid Crystal Display (LCD).

We get the definition of LCD from the name “Liquid Crystal” itself. It is actually a combination of two states of matter – the solid and the liquid. They have both the properties of solids and liquids and maintain their respective states with respect to another. Solids usually maintain their state unlike liquids who change their orientation and move everywhere in the particular liquid. Further studies have showed that liquid crystal materials show more of a liquid state than that of a solid. It must also be noted that liquid crystals are more heat sensitive than usual liquids. A little amount of heat can easily turn the liquid crystal into a liquid. This is the reason why they are also used to make thermometers.

Basics of LCD Displays:

The liquid-crystal display has the distinct advantage of having a low power consumption than the LED. It is typically of the order of microwatts for the display in comparison to the some order of milliwatts for LEDs. Low power consumption requirement has made it compatible with MOS integrated logic circuit. Its other advantages are its low cost, and good contrast. The main drawbacks of LCDs are additional requirement of light source, a limited temperature range of operation (between 0 and 60° C), low reliability, short operating life, poor visibility in low ambient lighting, slow speed and the need for an ac drive.

Basic structure of an LCD

A liquid crystal cell consists of a thin layer (about 10 u m) of a liquid crystal sandwiched between two glass sheets with transparent electrodes deposited on their inside faces. With both glass sheets transparent, the cell is known as transmittive type cell. When one glass is transparent and the other has a reflective coating, the cell is called reflective type. The LCD does not produce any illumination of its own. It, in fact, depends entirely on illumination falling on it from an external source for its visual effect

Types of LCD/Liquid Crystal Displays:

Two types of display available are dynamic scattering display and field effect display.

When dynamic scattering display is energized, the molecules of energized area of the display become turbulent and scatter light in all directions. Consequently, the activated areas take on a frosted glass appearance resulting in a silver display. Of course, the unenergized areas remain translucent.

Field effect LCD contains front and back polarizers at right angles to each other. Without electrical excitation, the light coming through the front polarizer is rotated 90° in the fluid.
Now, let us take a look at the different varieties of liquid crystals that are available for industrial purposes. The most usable liquid crystal among all the others is the nematic phase liquid crystals.

Nematic Phase LCD:

The greatest advantage of a nematic phase liquid crystal substance is that it can bring about predictable controlled changes according to the electric current passed through them. All the liquid crystals are according to their reaction on temperature difference and also the nature of the substance.
Twisted Nematics, a particular nematic substance is twisted naturally. When a known voltage is applied to the substance, it gets untwisted in varying degrees according to our requirement. This in turn is useful in controlling the passage of light. A nematic phase liquid crystal can be again classified on the basis in which the molecules orient themselves in respect to each other. This change in orientation mainly depends on the director, which can be anything ranging from a magnetic field to a surface with microscopic grooves. Classification includes Smectic and also cholesteric. Smectic can be again classified as smectic C, in which the molecules in each layer tilt at an angle from the previous layer. Cholesteric, on the other hand has molecules that twist slightly from one layer to the next, causing a spiral like design. There are also combinations of these two called Ferro-electric liquid crystals (FLC), which include cholesteric molecules in a smectic C type molecule so that the spiral nature of these molecules allows the microsecond switching response time. This makes FLCs to be of good use in advanced displays.
Liquid crystal molecules are further classified into thermotropic and lyotropic crystals. The former changes proportionally with respect to changes in pressure and temperature. They are further divided into nematic and isotropic. Nematic liquid crystals have a fixed order of pattern while isotropic liquid crystals are distributed randomly. The lyotropic crystal depends on the type of solvent they are mixed with. They are therefore useful in making detergents and soaps.

Making of LCD:

- Though the making of LCD is rather simple there are certain facts that should be noted while making it.
- The basic structure of an LCD should be controllably changed with respect to the applied electric current.
- The light that is used on the LCD can be polarized.
- Liquid crystals should be able to both transmit and change polarized light.
- There are transparent substances that can conduct electricity.

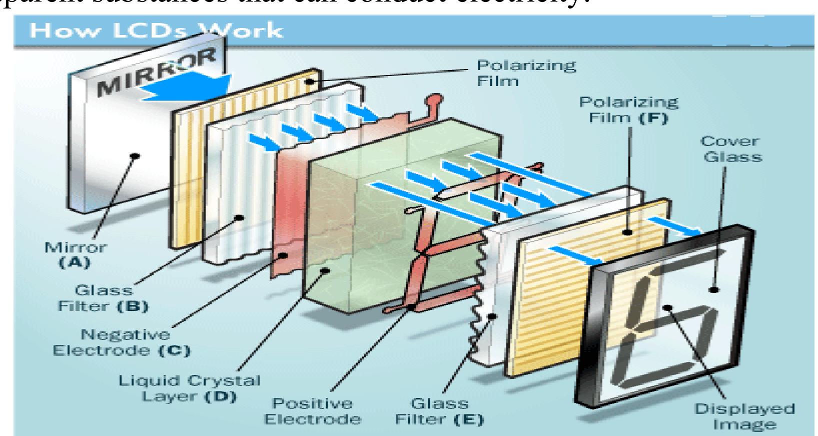


Figure 2.6: Working of LCD

To make an LCD, you need to take two polarized glass pieces. The glass which does not have a polarized film on it must be rubbed with a special polymer which creates microscopic grooves in the surface. It must also be noted that the grooves are on the same direction as the polarizing film. Then, all you need to do is to add a coating of nematic liquid crystals to one of the filters. The grooves will cause the first layer of molecules to align with the filter's orientation. At right angle to the first piece, you must then add a second piece of glass along with the polarizing film. Till the uppermost layer is at a 90-degree angle to the bottom, each successive layer of TN molecules will keep on twisting. The first filter will naturally be polarized as the light strikes it at the beginning. Thus the light passes through each layer and is guided on to the next with the help of molecules. When this happens, the molecules tend to change the plane of vibration of the light to match their own angle. When the light reaches the far side of the liquid crystal substance, it vibrates at the same angle as the final layer of molecules. The light is only allowed an entrance if the second polarized glass filter is same as the final layer. Take a look at the figure above.

Working of LCD:

The main principle behind liquid crystal molecules is that when an electric current is applied to them, they tend to untwist. This causes a change in the light angle passing through them. This causes a change in the angle of the top polarizing filter with respect to it. So little light is allowed to pass through that particular area of LCD. Thus that area becomes darker comparing to others.

For making an LCD screen, a reflective mirror has to be setup in the back. An electrode plane made of indium-tin oxide is kept on top and a glass with a polarizing film is also added on the bottom side. The entire area of the LCD has to be covered by a common electrode and above it should be the liquid crystal substance. Next comes another piece of glass with an electrode in the shape of the rectangle on the bottom and, on top, another polarizing film. It must be noted that both of them are kept at right angles. When there is no current, the light passes through the front of the LCD it will be reflected by the mirror and bounced back. As the electrode is connected to a temporary battery the current from it will cause the liquid crystals between the common-plane electrode and the electrode shaped like a rectangle to untwist. Thus the light is blocked from passing through. Thus that particular rectangular area appears blank.

Photodiode Theory of Operation:

A silicon photodiode is a solid-state device which converts incident light into an electric current. It consists of a shallow diffused p-n junction, normally a p-on-n configuration although "P-type" devices (n-on-p) are available for enhanced responsivity in the 1µm region. Modern day silicon photodiodes are generally made by planar diffusion or ion-implantation methods.

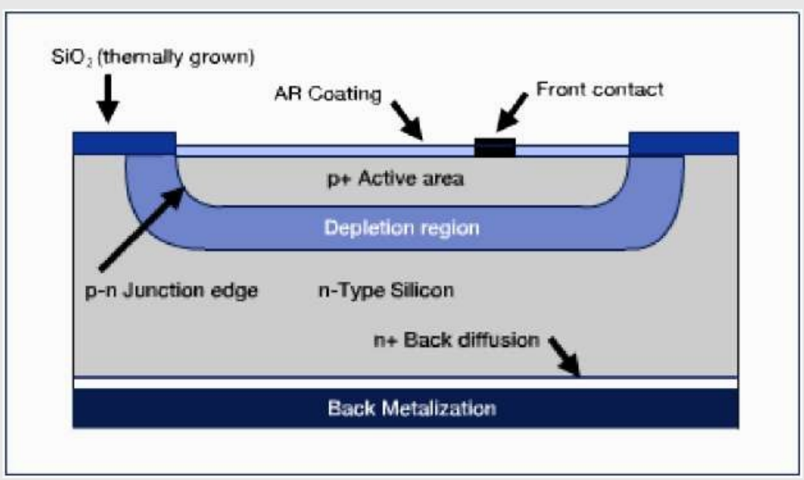


Figure 2.7: Operation of Photodiode

In the p-on-n planar diffused configuration, shown in the figure, the junction edge emerges on the top surface of the silicon chip, where it is passivated by a thermally grown oxide layer.

Basic photodiode physics:

The p-n junction and the depletion region are of major importance to the operation of a photodiode. These photodiode regions are created when the p-type dopant with acceptor impurities (excess holes), comes into contact with the n-type silicon, doped with donor impurities (excess electrons). The holes and the electrons, each experiencing a lower potential on the opposite side of the junction, begin to flow across the junction into their respective lower potential areas. This charge movement establishes a depletion region, which has an electric field opposite and equal to the low potential field, and hence no more current flows.

When photons of energy greater than 1.1eV (the bandgap of silicon) fall on the device, they are absorbed and electron-hole pairs are created. The depth at which the photons are absorbed depends upon their energy; the lower the energy of the photons, the deeper they are absorbed. The electron-hole pairs drift apart, and when the minority carriers reach the junction, they are swept across by the electric field. If the two sides are electrically connected, an external current flows through the connection. If the created minority carriers of that region recombine with the bulk carriers of that region before reaching the junction field, the carriers are lost and no external current flows.

The equivalent circuit of a photodiode is shown in the figure below. The photodiode behaves as a current source when illuminated. When operated without bias, this current is distributed between the internal shunt resistance and external load resistor. In this mode, a voltage develops which creates a forward bias, thus reducing its ability to remain a constant current source. When operated with a reverse voltage bias, the photodiode becomes an ideal current source.

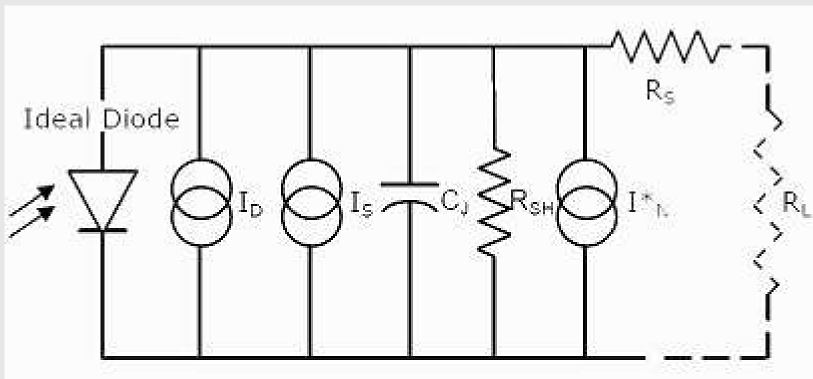


Figure 2.8: Equivalent Circuit of Photodiode

I_D = Dark current, Amps

I_S = Light Signal Current (I_S=RP_O)

R = Photodiode responsivity at wavelength of irradiance, Amps/Watt

P_O = Light power incident on photodiode active area, Watts

R_{SH} = Shunt Resistance, Ohms

I^*_N = Noise Current, Amps rms

C = Junction Capacitance, Farads

R_S = Series Resistance, Ohms

R_L = Load Resistance, Ohms

Silicon photodiodes are typically sensitive to light in the spectral range from about 200 nm (near UV) to about 1100 nm (near IR). Photosensor responsivity (R) is measured in Amperes (A) of photocurrent generated per Watt (W) of incident light power. Actual light levels in most applications typically range from picoWatts to milliWatts, which generate photocurrents from pico-Amps to milli-Amps. Responsivity in Amps/Watt varies with the wavelength of the incident light, with peak values from 0.4 to 0.7 A/W. The silicon photodiode response is well matched to light sources emitting in the UV to near infrared spectrum, such as HeNe lasers; GaAlAs and GaAs LEDs and laser diodes; and Nd:YAG lasers. Select a detector from the IR, Blue/Visible or UV series for a spectral response curve best matched to the spectral irradiance of your light source.

The silicon photodiode response is usually linear within a few tenths of a percent from the minimum detectable incident light power up to several milliWatts. Response linearity improves with increasing applied reverse bias and decreasing effective load resistance.

Heating the silicon photodiode shifts its spectral response curve (including the peak) toward longer wavelengths. Conversely, cooling shifts the response toward shorter wavelengths. The following values are typical for the temperature dependence of responsivity for different wavelength regions:-

UV to 500nm:	-0.1%/°C to -2%/°C
500 to 700nm:	~0%/°C
~900nm:	0.1 %/°C
1064 nm:	0.75%/°C to 0.9%/°C

Modes of operation:

A silicon photodiode can be operated in either the *photovoltaic* or *photoconductive* mode. In the photovoltaic mode, the photodiode is unbiased; while for the photoconductive mode, an external reverse bias is applied. Mode selection depends upon the speed requirements of the application, and the amount of dark current that is tolerable. In the photovoltaic mode, dark current is at a minimum. Photodiodes exhibit their fastest switching speeds when operated in the photoconductive mode.

Photodiodes and Op-Amps can be coupled such that the photodiode operates in a short circuit current mode. The op-amp functions as a simple current to voltage converter.

Varactor Diode:

Varactor Diode is a reverse biased p-n junction diode, whose capacitance can be varied electrically. As a result these diodes are also referred to as varicaps, tuning diodes, voltage variable capacitor diodes, parametric diodes and variable capacitor diodes. It is well known that the operation of the p-n junction depends on the bias applied which can be either forward or reverse in characteristic. It is also observed that the span of the depletion region in the p-n junction decreases as the voltage increases in case of forward bias. On the other hand, the width of the depletion region is seen to increase with an increase in the applied voltage for the reverse bias scenario. Under such condition, the p-n junction can be considered to be analogous to a capacitor (Figure 1) where the p and n layers represent the two plates of the capacitor while the depletion region acts as a

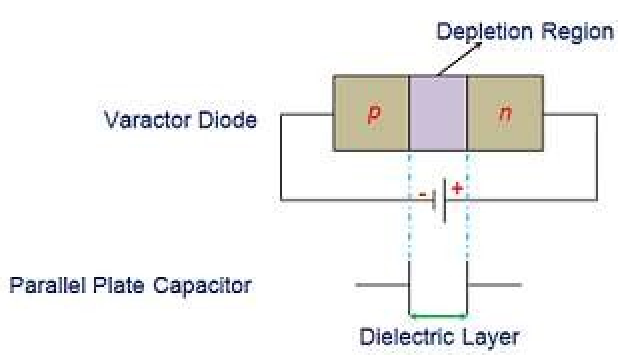


Figure 2.9: Varactor diode as Parallel plate

Dielectric separating them. Thus one can apply the formula used to compute the capacitance of a parallel plate capacitor even to the varactor diode.

Hence, mathematical expression for the capacitance of varactor diode is given by $C_j = \frac{\varepsilon A}{d}$

Where, C_j is the total capacitance of the junction. ε is the permittivity of the semiconductor material. A is the cross-sectional area of the junction. d is the width of the depletion region. Further the relationship between the capacitance and the reverse bias
voltage is given as

$$C_j = \frac{CK}{(V_b - V_R)^m}$$

Where, C_j is the capacitance of the varactor diode. C is the capacitance of the varactor diode when unbiased. K is the constant, often considered to be 1. V_b is the barrier potential. V_R is the applied reverse voltage. m is the material dependent constant. In addition, the electrical circuit equivalent of a **varactor diode** and its symbol are shown by Figure 2. This indicates that the maximum operating frequency of the circuit is dependent on the series resistance (R_s) and the diode capacitance, which can be mathematically given as

$$F = \frac{1}{2\pi R_s C_j}$$

In addition, the quality factor of the varactor diode is given by the equation

$$Q = \frac{F}{f}$$

Where, F and f represent the cut-off frequency and the operating frequency, respectively.

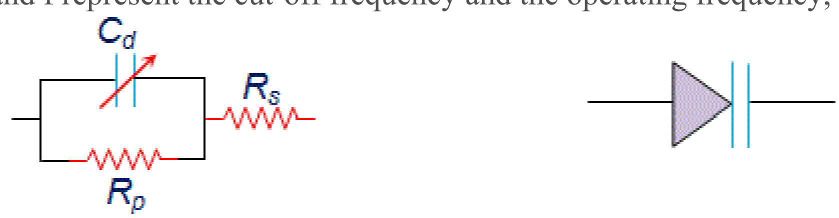


Figure 2.10; (a) Equivalent circuit of varactor diode (b) Symbolic representation

As a result, one can conclude that the capacitance of the varactor diode can be varied by varying the magnitude of the reverse bias voltage as it varies the width of the depletion region, d. Also it is evident from the capacitance equation that d is inversely proportional to C. This means that the junction capacitance of the **varactor diode** decreases with an increase in the depletion region width caused to due to an increase in the reverse bias voltage (V_R), as shown by the graph in Figure 3. Meanwhile it is important to note that although all the diodes exhibit the similar property, varactor diodes are specially manufactured to achieve the objective.

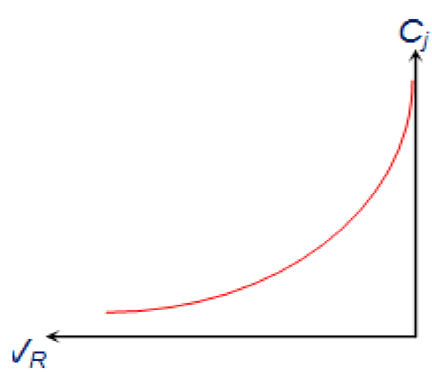


Figure 2.11: Characteristics of Varactor diode

In other words varactor diodes are manufactured with an intention to obtain a definite C-V curve which can be accomplished by controlling the level of doping during the process of manufacture. Depending on this, varactor diodes can be classified into two types viz., abrupt varactor diodes and hyper-abrupt varactor diodes, depending on whether the p-n junction diode is linearly or non-linearly doped (respectively).

These varactor diodes are advantageous as they are compact in size, economical, reliable and less prone to noise when compared to other diodes. Hence, they are used in

1. Tuning circuits to replace the old style variable capacitor tuning of FM radio
2. Small remote control circuits
3. Tank circuits of receiver or transmitter for auto-tuning as in case of TV
4. Signal modulation and demodulation.
5. Microwave frequency multipliers as a component of LC resonant circuit
6. Very low noise microwave parametric amplifiers
7. AFC circuits
8. Adjusting bridge circuits
9. Adjustable bandpass filters
10. Voltage Controlled Oscillators (VCOs)
11. RF phase shifters
12. Frequency multipliers

Tunnel Diode:

The application of transistors is very high in frequency range are hampered due to the transit time and other effects. Many devices use the negative conductance property of semiconductors for high frequency applications. Tunnel diode is one of the most commonly used negative conductance devices. It is also known as Esaki diode after L. Esaki for his work on this effect. This diode is a two terminal device. The concentration of dopants in both p and n region is very high. It is about 10^{24} - 10^{25} m^{-3} the p-n junction is also abrupt. For this reasons, the depletion layer width is very small. In the current voltage characteristics of tunnel diode, we can find a negative slope region when forward bias is applied. Quantum mechanical tunneling is responsible for the phenomenon and thus this device is named as tunnel diode.

The doping is very high so at absolute zero temperature the Fermi levels lies within the bias of the semiconductors. When no bias is applied any current flows through the junction.

Characteristics of Tunnel Diode

When reverse bias is applied the Fermi level of p - side becomes higher than the Fermi level of n-side. Hence, the tunneling of electrons from the balance band of p-side to the conduction band of n-side takes place. With the interments of the reverse bias the tunnel current also increases. When forward junction is a applied the Fermi level of n - side becomes higher that the Fermi level of p - side thus the tunneling of electrons from the n - side to p - side takes place. The amount of the tunnel current is very large than the normal junction current. When the forward bias is increased, the tunnel current is increased up to certain limit. When the band edge of n - side is same with the Fermi level in p - side the tunnel current is maximum with the further increment in the forward bias the tunnel current decreases and we get the desired negative conduction region. When the forward bias is raised further, normal p-n junction current is obtained which is exponentially proportional to the applied voltage. The V - I characteristics of the tunnel diode is given,

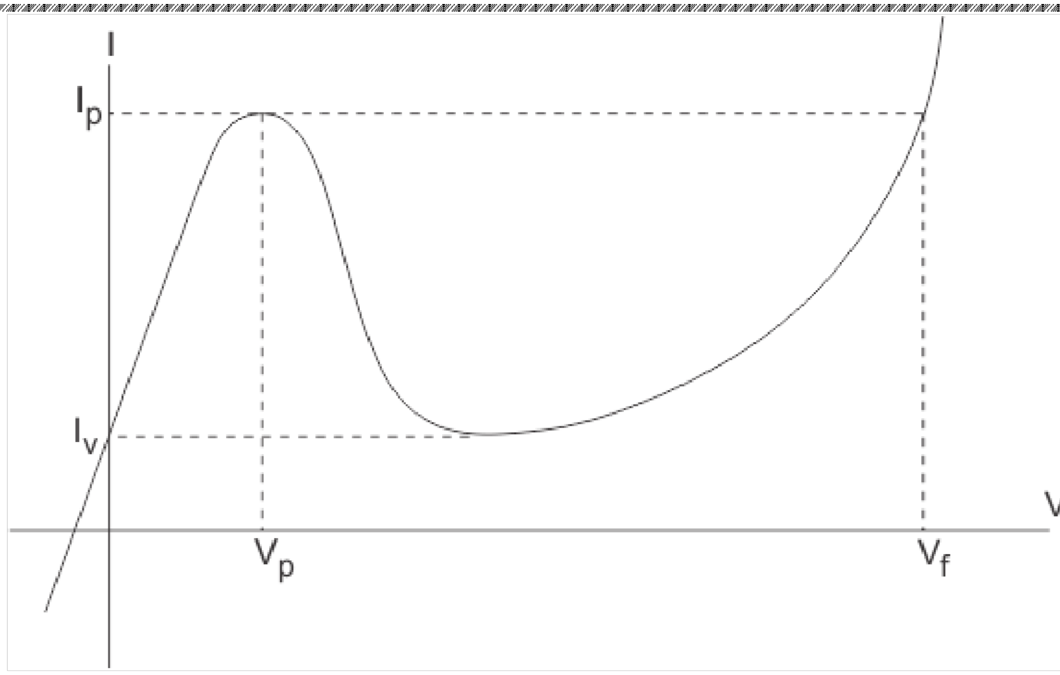


Figure 2.12: Characteristics of Tunnel diode

The negative resistance is used to achieve oscillation and often Ck+ function is of very high frequency frequencies.

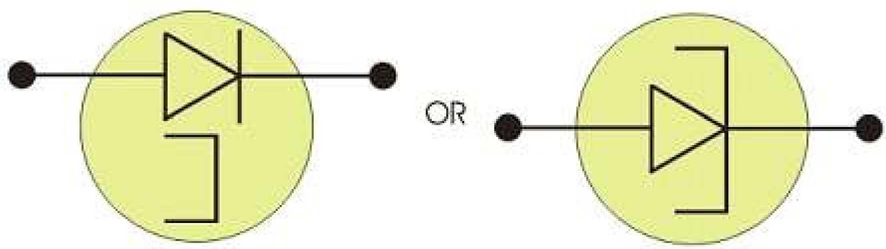


Figure 2.13: Symbol of Tunnel diode

Applications of Tunnel Diode:

Tunnel diode is a type of sc diode which is capable of very fast and in microwave frequency range. It was the quantum mechanical effect which is known as tunneling. It is ideal for fast oscillators and receivers for its negative slope characteristics. But it cannot be used in large integrated circuits – that's why it's an applications are limited.

SCR (Silicon Controlled Rectifier):

It is a four layered PNPN device and is a prominent member of thyristor family. It consists of three diodes connected back to back with gate connection or two complementary transistors connected back to back. It is widely used as switching device in power control applications. It can switch ON for variable length of time and delivers selected amount of power to load. It can control loads, by switching the current OFF and ON up to many thousand times a second. Hence it posses advantages of RHEOSTAT and a switch with none of their disadvantages.

Construction:

As shown in figure it is a four layered three terminal device. Layers being alternately P-type and N-type silicon. Junctions are marked $J_1J_2J_3$. Whereas terminals are anode (A), cathode (C) and gate (G). The gate terminal is connected to inner P-type layer and it controls the firing or switching of SCR.

Biasing:

The biasing of SCR is shown in figure . The junction J_1 and J_3 become forward biased while J_2 is reverse biased. In figure polarity is reversed. It is seen that now junction J_1 and J_3 become reverse biased and only J_2 is forward biased

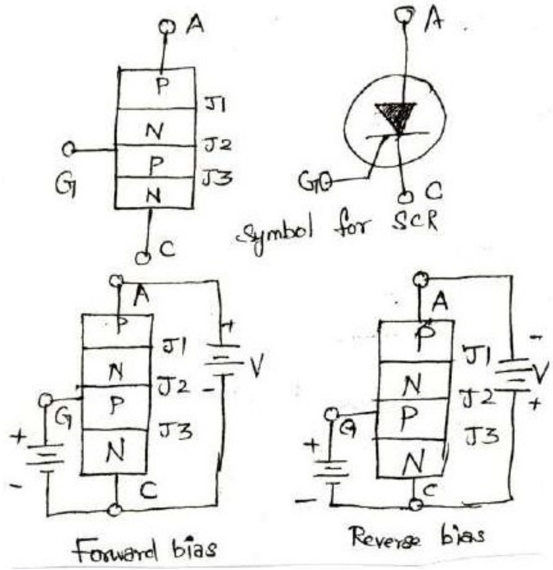


Figure 2.14: Circuit and Symbol of SCR

Operation of SCR:

- In SCR a load is connected in series with anode and is kept at positive potential with respect to cathode when the gate is open ile., no voltage is applied at the gate. Under this condition, junctions J_1 and J_3 are forward biased and junction J_2 is reverse biased. Due to this, no current flows through R_L and hence the SCR is cut off.
- However when the anode voltage is increased gradually to break over voltage, then breakdown occurs at junction J_2 due to this charge carriers are able to flow from cathode to anode easily, hence SCR starts conducting and is said to be in **ON state.** The SCR offers very small forward resistance so that it allow infinitely high current. The current flowing thorough the SCR is limited only by the anode voltage and external resistance.
- If the battery connections of the applied voltage are reversed as shown in figure the junction J_1 and J_3 are reverse biased. J_2 is forward biased. If the applied reverse voltage is small the **SCR is OFF** and hence no current flows through the device. If the reverse voltage is increased to reverse breakdown voltage, the junction J_1 and J_3 will breakdown due to avalanche effect. This causes current to flow through the SCR.
- From the above discussion we conclude that the SCR can be used to conduct only in forward direction. Therefore SCR is called as **"unidirectional device".**

V-I Characteristics of SCR:

The "**forward characteristics'** of SCR may be obtained using the figure. The volt-ampere characteristics of a SCR for I_G =0 is shown in figure.

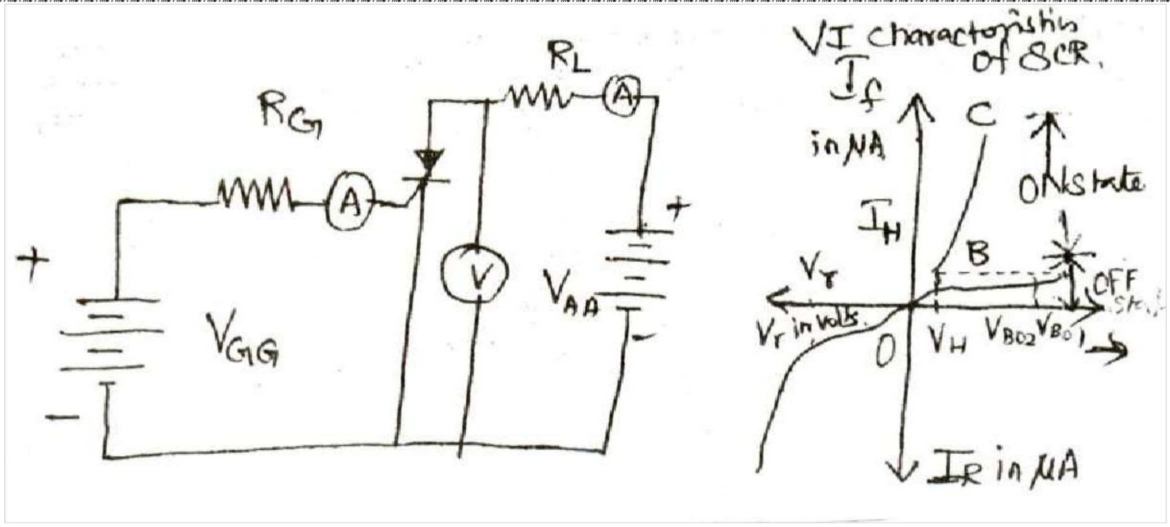


Figure 2.15: Circuit for V-I characteristics of SCR V_r in volts, V_{B01} for $I_0 = 0$, V_{B02} for I_G=1ma

1. As the applied anode to cathode voltage is increased above zero, a very small current flows through the device, under this condition the SCR is off. It will be continued until, the applied voltage the forward break over voltage (point A).
2. If the anode- cathode (applied) voltage exceeds the break over voltage it conducts heavily the SCR turn ON and anode to cathode voltage decreases quickly to a point B because, under this condition the SCR offers very low resistance hence it drops very low voltage across it.
3. At this stage is SCR allows more current to flow through it. The amplitude of the current is depending upon the supply voltage and load resistance connected in the circuit.
4. The current corresponding to the point 'B' is called the **"holding current (I_H)".** It can be defined as the minimum value of anode current required to keep the SCR in ON State. If the SCR falls below this holding current the SCR turns OFF.
5. If the value of the gate current I_G is increased above zero. (I_G >0) the SCR turns ON even at lower break over voltage as shown in figure.
6. The region lying between the points OA is called **forward blocking region.** In this region SCR is ON.
7. Once the SCR is switched ON then the gate looses all the control. So SCR cannot be turned OFF by varying the gate voltage. It is possible only by reducing the applied voltage.

To obtain the **"reverse characteristics"** the following points are followed.

1. In this case the SCR is reverse biased. If the applied reverse voltage is increased above zero, hence a very small current flows through the SCR. Under this condition the SCR is OFF, it continues till the applied reverse voltage reaches breakdown voltage.
2. As the applied reverse voltage is increased above the breakdown voltage, the avalanche breakdown occurs hence SCR starts conducting in the reverse direction. It is shown in curve DE. Suppose the applied voltage is increased to a very high value, the device may get damaged.

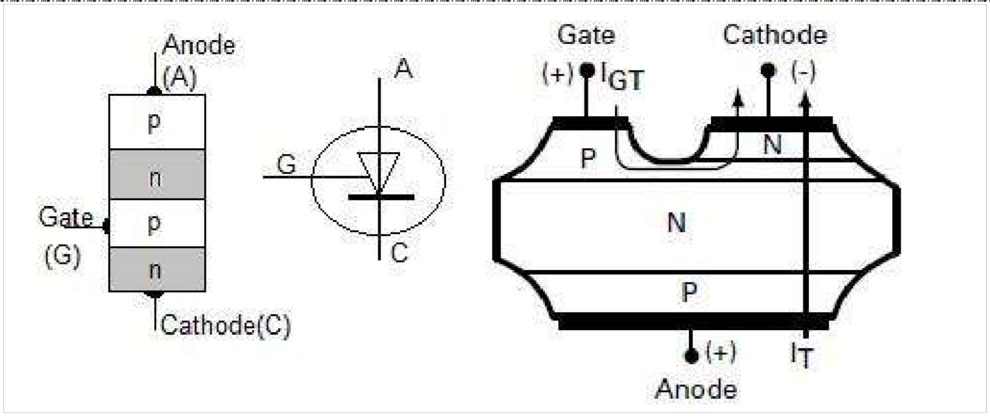


Figure 2.16: Structure and symbol of SCR

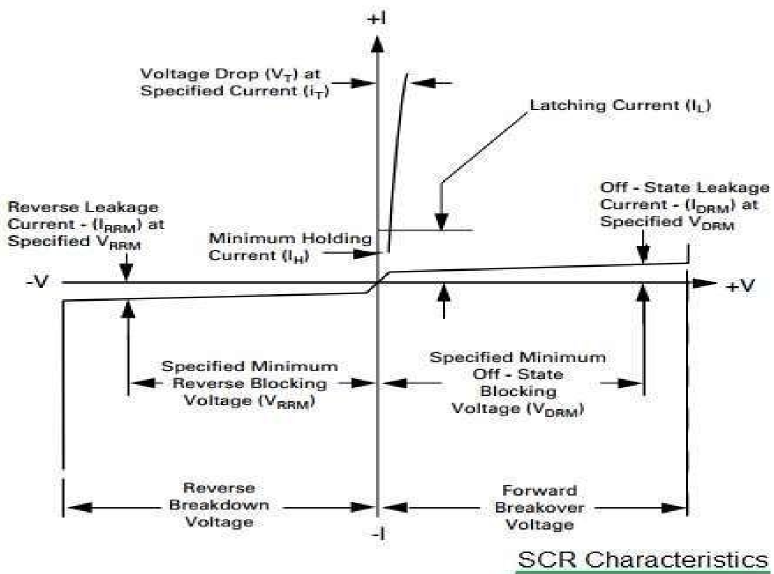


Figure 2.17: Characteristics of SCR

The full form of SCR is Silicon Controlled Rectifier.

- It is a three terminal device.
- It has 4 layers of semiconductor.
- It is a unidirectional switch. It conducts current only in one direction. Hence it can control DC power only OR it can control forward biased half cycle of AC input in the load.
- Basically SCR can only control either positive or negative half cycle of AC input.

<u>TRIAC:</u>

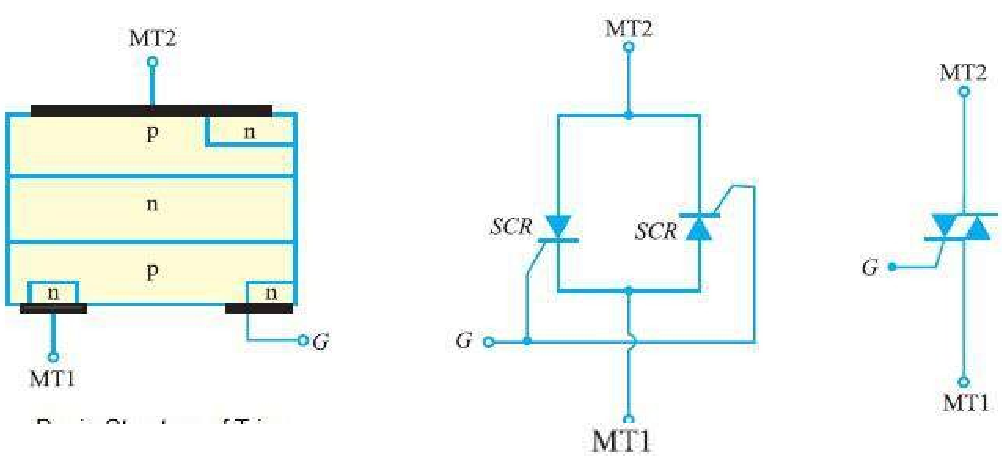


Figure 2.18: (a) Basic Structure of TRIAC (b) SCR equivalent of TRIAC (c) Symbol of TRIAC

It is a 5-layer 3 terminal "bidirectional device" which can be triggered ON by applying either positive or negative voltages irrespective of the polarity of the voltage across the terminal anodes (A_1, A_2) and gate… It behaves like two SCR's, connected in parallel and in opposite direction to each other. Because of the inverse parallel and in opposite direction to each other as anode or cathode. The anode and gate voltage applied in either direction will fire (ON) a triac because they would fire at least one of the two SCR's which are in opposite directions.

Construction:

It has three terminals A_1,A_2 and G. The gate G is closer to anode A_1. It has six doped regions. It is nothing but two inverse parallel connected SCR's with common gate terminal. The schematic symbol of Triac is shown in operation.

- When positive voltage is applied to A_2, with respect to A_1 path of current flow is P_1-N_1-P_2-N_2. The two junction P_1-N_1 and P_2-N_2 are forward biased whereas N_1-P_2 junction is blocked. The gate can be given either positive or negative voltage to turn on the triac.

(i) **Positive gate:** The positive gate forward biases the P_2-N_2 junction and breakdown occurs as in normal SCR.

(ii) **Negative gate:** A negative gate forward biases the P_2-N_3 junction and current carriers are injected into P_2 to turn on the triac.

- When positive voltage is applied to anode A_1, path of current flow is P_2-N_1-P_1-N_4.The two junctions P_2-N_1 and P_1-N_4 are forward biased whereas junction N_1-P_1 is blocked. Conduction can be achieved by applying either positive or negative voltage to G.

(i) **Positive Gate:** A positive gate injects current carriers by forward biasing P_2-N_2 junction and thus initializes conduction.

(ii) **Negative Gate :** A negative gate injects current carriers by forward biasing P_2-N_3 junction, thereby triggering conduction. Thus there are four TRIAC triggering mode, two for each of two anodes.

V-I Characteristics:

- As seen in SCR, triac exhibits same forward blocking and forward conducting characteristics like SCR but for either polarity of voltage applied to main terminal. Triac has latch current in either direction hence the switching ON is effected by raising the applied voltage to break over voltage. The triac can be made to conduct in either direction. No matter what bias polarity. characteristic of triac are those of forward biased SCR.
- If the applied voltage to one of the main terminal is increased above zero, a very small current flows through the device, under this condition the triac is OFF, it will be continued until the applied voltage reaches the forward break over voltage(point) A.
- If the anode to cathode voltage exceeds the break over voltage, the SCR turns ON and anode to cathode voltage decreases quickly to point 'B", because under this conditions the SCR offers very low resistance hence It drops very low voltage across it. At this stage the SCR allows more current to flow through it, The amplitude of the current is depending upon the supply voltage and load resistance connected in the circuit.
- The same procedure is repeated for forward blocking state with the polarity of main terminals interchanged. The VI characteristics is shown in figure.

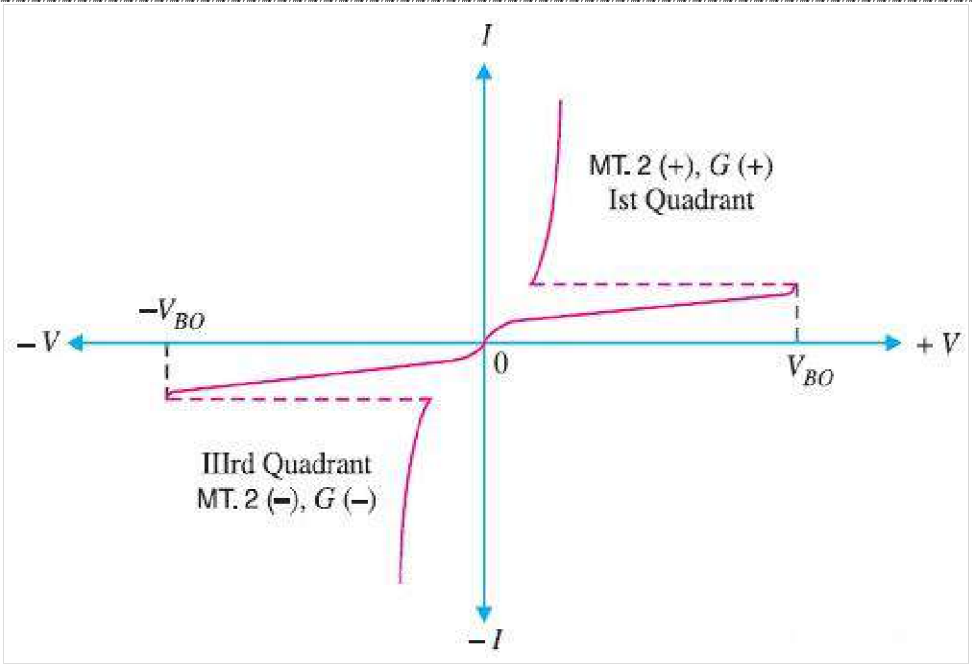


Figure 2.19: V-I Characteristics of TRIAC

• The name "TRIAC" is derived from combination of "TRI" means three and "AC" or alternating current.
• It is a three terminal semiconductor device.
• It has 5 layers of semiconductor.
• It can control both positive and negative half cycles of AC signal input.
• It is a bidirectional switch.
• The forward and reverse characteristics of TRIAC is similar to forward characteristics of SCR device.
• Construction of TRIAC is equivalent to 2 separate SCR devices connected in inverse parallel as shown in the figure.
• Similar to the SCR, once the triac is fired into conduction, the gate will lose all the control. At this stage, the TRIAC can be turned OFF by reducing current in the circuit below the holding value of current.
• The main demerit of TRIAC over SCR is that TRIAC has lower current capabilities. Typically most of the TRIACs are available in ratings less than 40 Amp and at voltages upto 600 Volt.
Figure 2.19 depicts V-I characteristics of TRIAC. Following can be derived from TRIAC characteristics.
• V-I characteristics in first and third quadrants are same except direction of voltage and current flow. This characteristic in the 1st and 3rd quadrant is identical to SCR characteristic in the 1st quadrant.
• TRIAC can function with either positive(+ve) or negative(-ve) gate control voltage. In normal operation, gate voltage is +ve in 1st quadrant and -ve in 3rd quadrant.

DIAC:

A diac is a two terminal, three layer bidirectional device which can be switched from its OFF state to ON state for either polarity of applied voltage Figure 16(a) shows the basic structure of a DIAC. The two leads are connected to P-region of silicon chip separated by an N- region. MT_1 and MT_2 are two main terminals by which the structure of the diac in interchangeable. It is like a transistor with the following basic differences.

(i) There is no terminal attached to the base layer
(ii) The doping concentrations are identical (unlike a bipolar transistor)to give the device symmetrical properties.

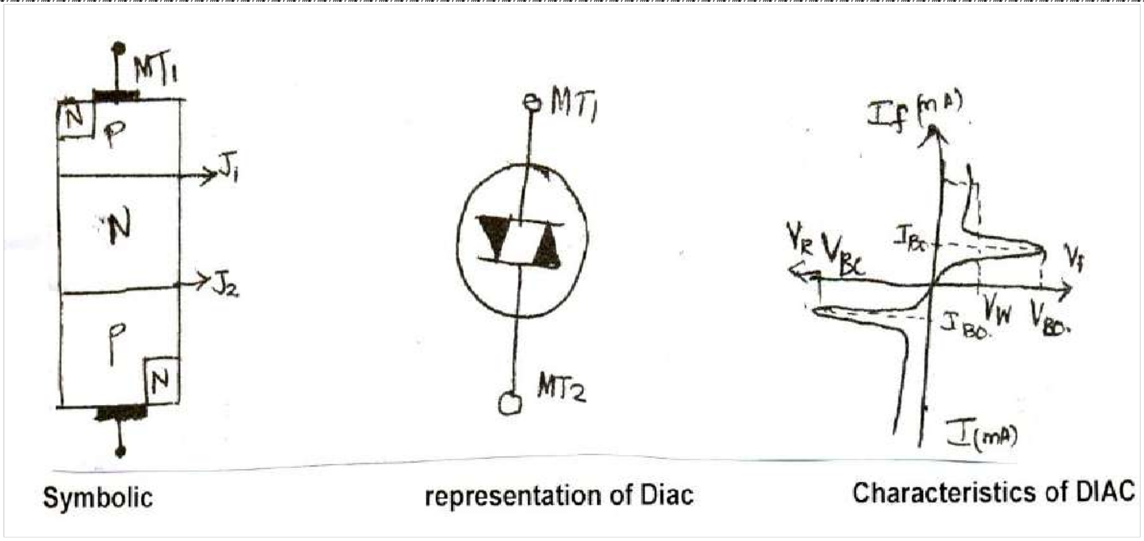


Figure 2.20: **Symbol, representation & V-I characteristics of DIAC**

Operation:

When a positive or negative voltage is applied across the main terminals of a diac, only a small leakage current I_{B0} will flow through the device. If the applied voltage is increased, the lead age current will continue to flow until the voltage reaches the break over voltage V_{BO}. At this point avalanche breakdown occurs at the reverse-biased junction it may be J_1 or J_2 depending upon the supply connected between MT_1 &MT_2 and the device exhibits negative resistance i.e current through the device increases with the decreasing values of applied voltage. The voltage across the device then drops to ‘break back” voltage V_w

V-I Characteristics of DIAC:

The figure 2.20 shows the VI Characteristics of diac . If the applied (positive or negative) voltage is less the V_{BO} a small leakage current (I_{B0}) flows through the device. Under this conditions, the diac blocks the flow of current and effectively behaves as an open circuit. The voltage V_{Bo} is the break over voltage and usually have a range of 30 to 50 volts.

When the (positive or negative) voltage applied to diac is equal to or greater than the break over voltage then diac begins to conduct, due to avalanche breakdown of the reverse biased junction and the voltage drop across it becomes a few volt, result in which the diac current increases sharply and the volt across the diac decreases as shown in figure 16.Thus the diac offers a **negative resistance.**

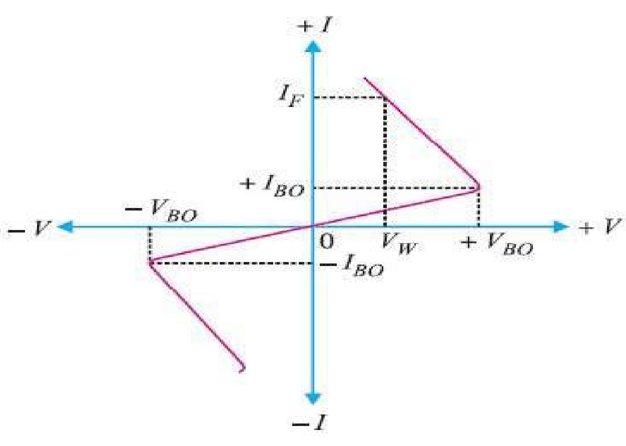


Figure 2.21: V-I characteristics of DIAC

Applications of DIAC:

Some of the circuit application of diac are

(i) Light dimmer circuits
(ii) Heat control circuits
(iii) Universal motor speed control.

• It is a two terminal device.
• It is 3 layer bidirectional device.
• Diac can be switched from its off state to ON state for either polarity of applied voltage.
• The DIAC can be made either in PNP or NPN structure form. The figure depicts DIAC in PNP form which has two p-regions of silicon separated by n-region.

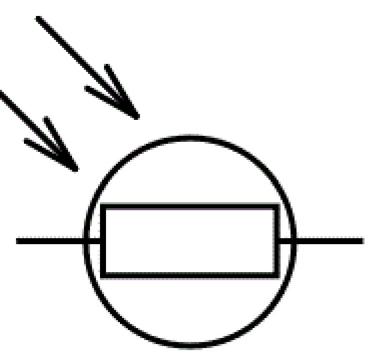
Let us compare DIAC vs TRANSISTOR and understand similarities and difference between DIAC and TRANSISTOR.

• Structure of DIAC is similar to the structure of transistor.
• There is no terminal attached with base layer in DIAC unlike transistor.
• All the three regions in DIAC are identical in size unlike transistor.
• The doping concentrations are identical in these three regions in DIAC unlike bipolar transistor. This will give DIAC device symmetrical properties.

Light Dependent Resistor or a Photo Resistor:

A ***Light Dependent Resistor*** (LDR) or a photo resistor is a device whose resistivity is a function of the incident electromagnetic radiation. Hence, they are light sensitive devices. They are also called as photo conductors, photo conductive cells or simply photocells.

They are made up of semiconductor materials having high resistance. There are many different symbols used to indicate a **LDR**, one of the most commonly used symbol is shown in the figure below. The arrow



indicates light falling on it.

Figure 2.22: Symbol of LDR

Working Principle of LDR:

A **light dependent resistor** works on the principle of photo conductivity. Photo conductivity is an optical phenomenon in which the materials conductivity is increased when light is absorbed by the material. When light falls i.e. when the photons fall on the device, the electrons in the valence band of the semiconductor material are excited to the conduction band. These photons in the incident light should have energy greater than the band gap of the semiconductor material to make the electrons jump from the valence band to the conduction band. Hence when light having enough energy strikes on the device, more and more electrons are excited to the conduction band which results in large number of charge carriers. The result of this process is more and more current starts flowing through the device when the circuit is closed and hence it is said that the resistance of the device has been decreased. This is the most common **working principle of LDR**.

Characteristics of LDR:

LDR's are light dependent devices whose resistance is decreased when light falls on them and that is increased in the dark. When a **light dependent resistor** is kept in dark, its resistance is very high. This resistance is called as dark resistance. It can be as high as $10^{12}\ \Omega$ and if the device is allowed to absorb light its resistance will be decreased drastically. If a constant voltage is applied to it and intensity of light is increased the current starts increasing. Figure below shows resistance vs. illumination curve for a particular **LDR**.

Photocells or LDR's are non linear devices. There sensitivity varies with the wavelength of light incident on them. Some photocells might not at all response to a certain range of wavelengths. Based on the material used different cells have different spectral response curves.

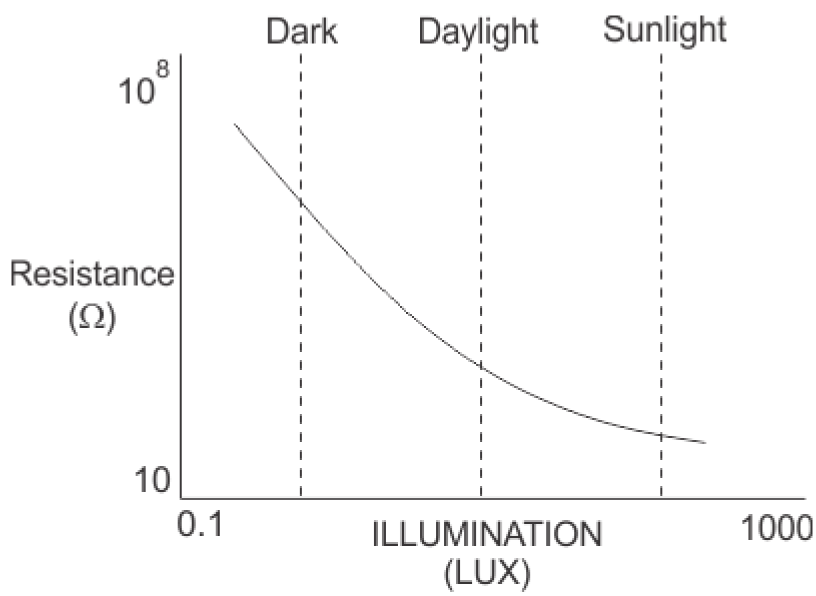


Figure 2.23: Characteristics of LDR

When light is incident on a photocell it usually takes about 8 to 12 ms for the change in resistance to take place, while it takes one or more seconds for the resistance to rise back again to its initial value after removal of light. This phenomenon is called as resistance recovery rate. This property is used in audio compressors. Also, **LDR**'s are less sensitive than photo diodes and phototransistor. (A photo diode and a photocell (LDR) are not the same, a photo-diode is a pn junction semiconductor device that converts light to electricity, whereas a photocell is a passive device, there is no pn junction in this nor it "converts" light to electricity).

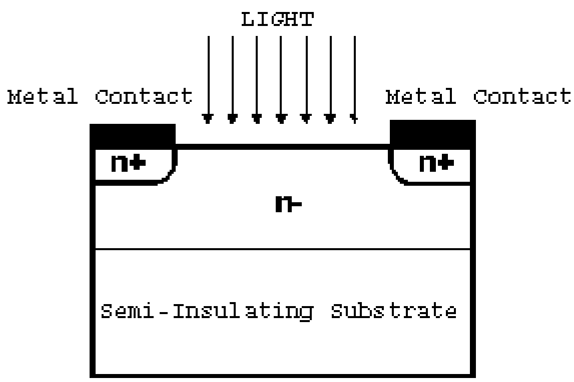
Types of Light Dependent Resistors:

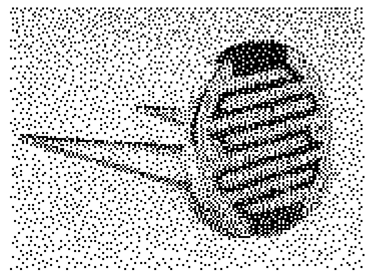
Based on the materials used they are classified as:

1. **Intrinsic photo resistors (Un doped semiconductor):** These are made of pure semiconductor materials such as silicon or germanium. Electrons get excited from valance band to conduction band when photons of enough energy fall on it and number charge carriers is increased.
2. **Extrinsic photo resistors:** These are semiconductor materials doped with impurities which are called as dopants. Theses dopants create new energy bands above the valence band which are filled with electrons. Hence this reduces the band gap and less energy is required in exciting them. Extrinsic photo resistors are generally used for long wavelengths.

Construction of a Photocell:

The structure of a **light dependent resistor** consists of a light sensitive material which is deposited on an insulating substrate such as ceramic. The material is deposited in zigzag pattern in order to obtain the desired resistance and power rating. This zigzag area separates the metal deposited areas into two regions. Then the ohmic contacts are made on the either sides of the area. The resistances of these contacts should be as less as possible to make sure that the resistance mainly changes due to the effect of light only. Materials normally used are cadmium sulphide, cadmium selenide, indium antimonide and cadmium sulphonide. The use of lead and cadmium is avoided as they are harmful to the environment.





Applications of LDR:

LDR's have low cost and simple structure. They are often used as light sensors. They are used when there is a need to detect absences or presences of light like in a camera light meter. Used in street lamps, alarm clock, burglar alarm circuits, light intensity meters, for counting the packages moving on a conveyor belt, etc.

Photovoltaic Cell:

Conversion of light energy in electrical energy is based on a phenomenon called photovoltaic effect. When semiconductor materials are exposed to light, the some of the photons of light ray are absorbed by the semiconductor crystal which causes a significant number of free electrons in the crystal. This is the basic reason for producing electricity due to photovoltaic effect. **Photovoltaic cell** is the basic unit of the system where the photovoltaic effect is utilised to produce electricity from light energy. Silicon is the most widely used semiconductor material for constructing the photovoltaic cell. The silicon atom has four valence electrons. In a solid crystal, each silicon atom shares each of its four valence electrons with another nearest silicon atom hence creating covalent bonds between them. In this way, silicon crystal gets a tetrahedral lattice structure. While light ray strikes on any materials some portion of the light is reflected, some portion is transmitted through the materials and rest is absorbed by the materials.

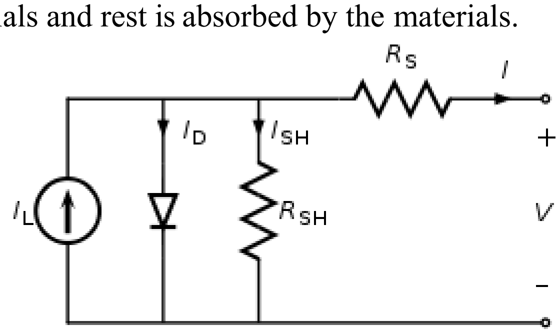


Figure 2.24: Equivalent circuit of PV Cell

The same thing happens when light falls on a silicon crystal. If the intensity of incident light is high enough, sufficient numbers of photons are absorbed by the crystal and these photons, in turn, excite some of the electrons of covalent bonds. These excited electrons then get sufficient energy to migrate from valence band to conduction band. As the energy level of these electrons is in the conduction band, they leave from the covalent bond leaving a hole in the bond behind each removed electron. These are called free electrons move randomly inside the crystal structure of the silicon. These free electrons and holes have a vital role in creating electricity in **photovoltaic cell**. These electrons and holes are hence called **light-generated electrons and holes** respectively. These light generated electrons and holes cannot produce electricity in the silicon crystal alone. There should be some additional mechanism to do that.

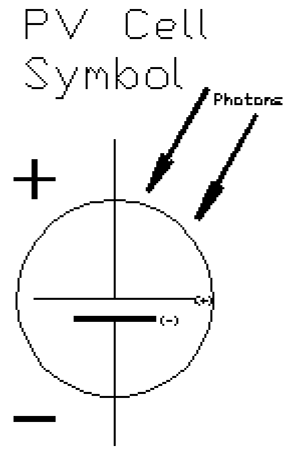


Figure 2.24: Symbol of PV Cell

When a pentavalent impurity such as phosphorus is added to silicon, the four valence electrons of each pentavalent phosphorous atom are shared through covalent bonds with four neighbour silicon atoms, and fifth valence electron does not get any chance to create a covalent bond.

This fifth electron then relatively loosely bounded with its parent atom. Even at room temperature, the thermal energy available in the crystal is large enough to disassociate these relatively loose fifth electrons from their parent phosphorus atom. While this fifth relatively loose electron is disassociated from parent phosphorus atom, the phosphorous atom immobile positive ions. The said disassociated electron becomes free but does not have any incomplete covalent bond or hole in the crystal to be re-associated. These free electrons come from pentavalent impurity are always ready to conduct current in the semiconductor. Although there are numbers of free electrons, still the substance is electrically neutral as the number of positive phosphorous ions locked inside the crystal structure is exactly equal to the number of the free electrons come out from them. The process of inserting impurities in the semiconductor is known as doping, and the impurities are doped are known as dopants. The pentavalent dopants which donate their fifth free electron to the semiconductor crystal are known as donors. The semiconductors doped by donor impurities are known as n-type or negative type semiconductor as there are plenty of free electrons which are negatively charged by nature.

When instead pentavalent phosphorous atoms, trivalent impurity atoms like boron are added to a semiconductor crystal opposite type of semiconductor will be created. In this case, some silicon atoms in the crystal lattice will be replaced by boron atoms, in other words, the boron atoms will occupy the positions of replaced silicon atoms in the lattice structure. Three valance electrons of boron atom will pair with valance electron of three neighbour silicon atoms to create three complete covalent bonds. For this configuration, there will be a silicon atom for each boron atom, fourth valence electron of which will not find any neighbour valance electrons to complete its fourth covalent bond. Hence this fourth valence electron of these silicon atoms remains unpaired and behaves as incomplete bond. So there will be lack of one electron in the incomplete bond, and hence an incomplete bond always attracts electron to fulfil this lack. As such, there is a vacancy for the electron to sit.

This vacancy is conceptually called positive hole. In a trivalent impurity doped semiconductor, a significant number of covalent bonds are continually broken to complete other incomplete covalent bonds. When one bond is broken one hole is created in it. When one bond is completed, the hole in it disappears. In this way, one hole appears to disappear another neighbour hole. As such holes are having relative motion inside the semiconductor crystal. In the view of that, it can be said holes also can move freely as free electrons inside semiconductor crystal. As each of the holes can accept an electron, the trivalent impurities are known as acceptor dopants and the semiconductors doped with acceptor dopants are known as p-type or positive type semiconductor.

In n-type semiconductor mainly the free electrons carry negative charge and in p-type semiconductor mainly the holes in turn carry positive charge therefore free electrons in n-type semiconductor and free holes in p-type semiconductor are called majority carrier in n-type semiconductor and p-type semiconductor respectively.

There is always a potential barrier between n-type and p-type material. This potential barrier is essential for working of a photovoltaic or solar cell. While n-type semiconductor and p-type semiconductor contact each other, the free electrons near to the contact surface of n-type semiconductor get plenty of adjacent holes of p-type material. Hence free electrons in n-type semiconductor near to its contact surface jump to the adjacent holes of p-type material to recombine. Not only free electrons, but valence electrons of n-type material near the contact surface also come out from the covalent bond and recombine with more nearby holes in the p-type semiconductor. As the covalent bonds are broken, there will be a number of holes created in the n-type material near the contact surface. Hence, near contact zone, the holes in the p-type materials disappear due to recombination on the other hand holes appear in the n-type material near same contact zone. This is as such equivalent to the migration of holes from p-type to the n-type semiconductor. So as soon as one n-type semiconductor and one p-type semiconductor come into contact the electrons from n-type will transfer to p-type and holes from p-type will transfer to n-type. The process is very fast but does not continue forever. After some instant, there will be a layer of negative charge (excess electrons) in the p-type semiconductor adjacent to the contact along the contact surface. Similarly, there will be a layer of positive charge (positive ions) in the n-type semiconductor adjacent to contact along the contact surface. The thickness of these negative and positive charge layer increases up to a certain extent, but after that, no more electrons will migrate from n-type semiconductor to p-type semiconductor. This is because, while any electron of n-type semiconductor tries to migrate over p-type semiconductor it faces a sufficiently thick layer of positive ions in n-type semiconductor itself where it will drop without crossing it. Similarly, holes will no more migrate to n-type semiconductor from p-type. The holes when trying to cross the negative layer in p-type semiconductor these will recombine with electrons and no more movement toward n-type region.

In other words, negative charge layer in the p-type side and positive charge layer in n-type side together form a barrier which opposes migration of charge carriers from its one side to other. Similarly, holes in the p-type region are held back from entering the n-type region. Due to positive and negative charged layer, there will be an electric field across the region and this region is called depletion layer.

Now let us come to the silicon crystal. When light ray strikes on the crystal, some portion of the light is absorbed by the crystal, and consequently, some of the valence electrons are excited and come out from the covalent bond resulting free electron-hole pairs.

If light strikes on n-type semiconductor the electrons from such light-generated electron-hole pairs are unable to migrate to the p-region since they are not able to cross the potential barrier due to the repulsion of an electric field across depletion layer. At the same time, the light-generated holes cross the depletion region due to the attraction of electric field of depletion layer where they recombine with electrons, and then the lack of electrons here is compensated by valence electrons of p-region, and this makes as many numbers of

holes in the p-region. As such light generated holes are shifted to the p-region where they are trapped because once they come to the p-region cannot be able to come back to n-type region due to the repulsion of potential barrier.
As the negative charge (light generated electrons) is trapped in one side and positive charge (light generated holes) is trapped in opposite side of a cell, there will be a potential difference between these two sides of the cell. This potential difference is typically 0.5 V. This is how a **photovoltaic cells** or **solar cells** produce potential difference.

Schottky diode:

Schottky diode is a metal-semiconductor junction diode that has less forward voltage drop than the P-N junction diode and can be used in high-speed switching applications. In a normal p-n junction diode, a p-type semiconductor and an n-type semiconductorare used to form the p-n junction. When a p-type semiconductor is joined with an n-type semiconductor, a junction is formed between the P-type and N-type semiconductor. This junction is known as P-N junction. In schottky diode, metals such as aluminum or platinum replace the P-type semiconductor. The schottky diode is named after German physicist Walter H. Schottky.Schottky diode is also known as schottky barrier diode, surface barrier diode, majority carrier device, hot-electron diode, or hot carrier diode. Schottky diodes are widely used in radio frequency (RF) applications.When aluminum or platinum metal is joined with N-type semiconductor, a junction is formed between the metal and N-type semiconductor. This junction is known as a metal-semiconductor junction or M-S junction. A metal-semiconductor junction formed between a metal and n-type semiconductor creates a barrier or depletion layer known as a schottky barrier.Schottky diode can switch on and off much faster than the p-n junction diode. Also, the schottky diode produces less unwanted noise than p-n junction diode. These two characteristics of the schottky diode make it very useful in high-speed switching power circuits.

When sufficient voltage is applied to the schottky diode, current starts flowing in the forward direction. Because of this current flow, a small voltage loss occurs across the terminals of the schottky diode. This voltage loss is known as voltage drop.
A silicon diode has a voltage drop of 0.6 to 0.7 volts, while a schottky diode has a voltage drop of 0.2 to 0.3 volts. Voltage loss or voltage drop is the amount of voltage wasted to turn on a diode.
In silicon diode, 0.6 to 0.7 volts is wasted to turn on the diode, whereas in schottky diode, 0.2 to 0.3 volts is wasted to turn on the diode. Therefore, the schottky diode consumes less voltage to turn on.
The voltage needed to turn on the schottky diode is same as that of a germanium diode. But germanium diodes are rarely used because the switching speed of germanium diodes is very low as compared to the schottky diodes.

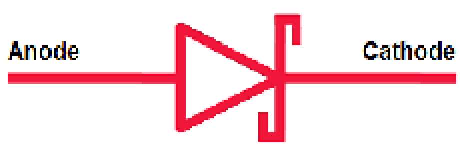


Figure 2.25: Symbol of Schottky Diode

Working of schottky diode:

When the metal is joined with the n-type semiconductor, the conduction band electrons (free electrons) in the n-type semiconductor will move from n-type semiconductor to metal to establish an equilibrium state.
We know that when a neutral atom loses an electron it becomes a positive ion similarly when a neutral atom gains an extra electron it becomes a negative ion.
The conduction band electrons or free electrons that are crossing the junction will provide extra electrons to the atoms in the metal. As a result, the atoms at the metal junction gains extra electrons and the atoms at the n-side junction lose electrons.
The atoms that lose electrons at the n-side junction will become positive ions whereas the atoms that gain extra electrons at the metal junction will become negative ions. Thus, positive ions are created the n-side

junction and negative ions are created at the metal junction. These positive and negative ions are nothing but the depletion region.

Since the metal has a sea of free electrons, the width over which these electrons move into the metal is negligibly thin as compared to the width inside the n-type semiconductor. So the built-in-potential or built-in-voltage is primarily present inside the n-type semiconductor. The built-in-voltage is the barrier seen by the conduction band electrons of the n-type semiconductor when trying to move into the metal.

To overcome this barrier, the free electrons need energy greater than the built-in-voltage. In unbiased schottky diode, only a small number of electrons will flow from n-type semiconductor to metal. The built-in-voltage prevents further electron flow from the semiconductor conduction band into the metal.

The transfer of free electrons from the n-type semiconductor into metal results in energy band bending near the contact.

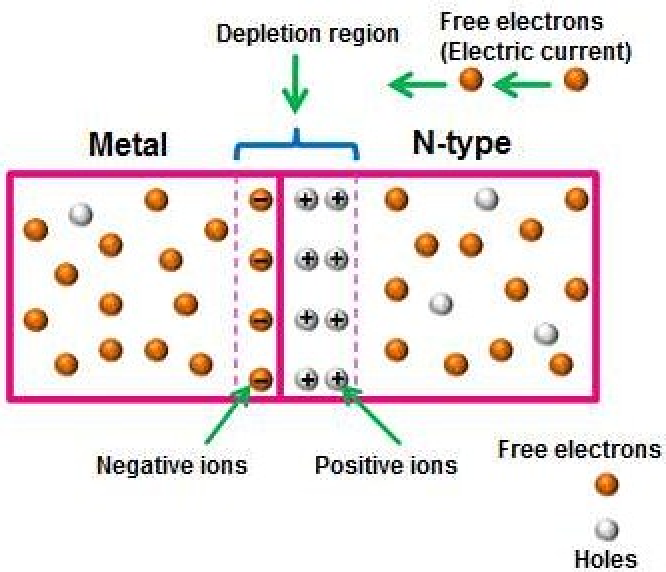


Figure 2.25: Unbiased of Schottky Diode

<u>Forward biased schottky diode:</u>

If the positive terminal of the battery is connected to the metal and the negative terminal of the battery is connected to the n-type semiconductor, the schottky diode is said to be forward biased.

When a forward bias voltage is applied to the schottky diode, a large number of free electrons are generated in the n-type semiconductor and metal. However, the free electrons in n-type semiconductor and metal cannot cross the junction unless the applied voltage is greater than 0.2 volts.

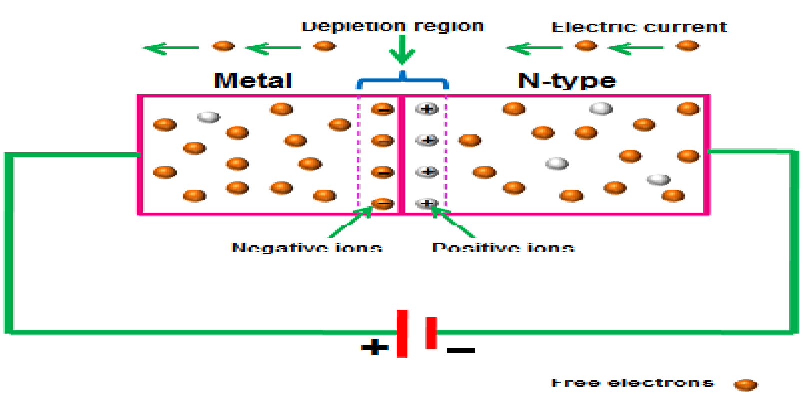


Figure 2.26: Forward biased Schottky Diode

If the applied voltage is greater than 0.2 volts, the free electrons gain enough energy and overcomes the built-in-voltage of the depletion region. As a result, electric current starts flowing through the schottky diode.

If the applied voltage is continuously increased, the depletion region becomes very thin and finally disappears.

Reverse bias schottky diode:

If the negative terminal of the battery is connected to the metal and the positive terminal of the battery is connected to the n-type semiconductor, the schottky diode is said to be reverse biased.
When a reverse bias voltage is applied to the schottky diode, the depletion width increases. As a result, the electric current stops flowing. However, a small leakage current flows due to the thermally excited electrons in the metal.

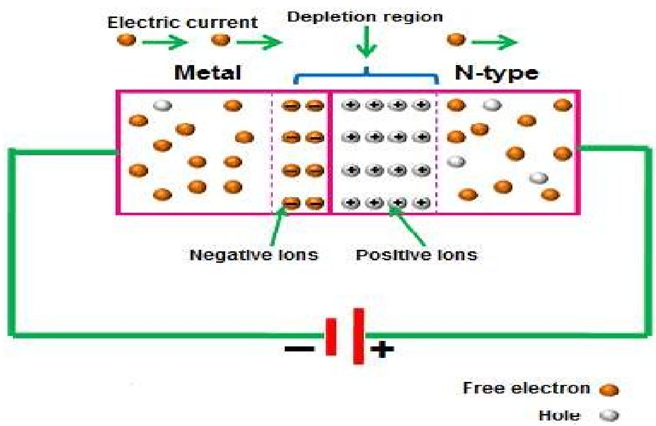


Figure 2.27: Reverse biased Schottky Diode

If the reverse bias voltage is continuously increased, the electric current gradually increases due to the weak barrier.If the reverse bias voltage is largely increased, a sudden rise in electric current takes place. This sudden rise in electric current causes depletion region to break down which may permanently damage the device.

V-I characteristics of schottky diode:

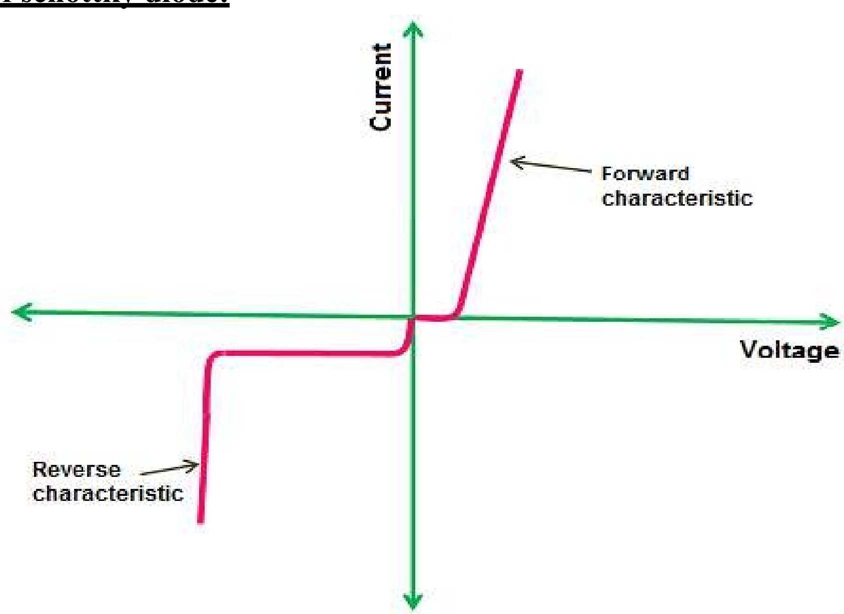


Figure 2.27: V-I characteristics of Schottky Diode

The V-I (Voltage-Current) characteristics of schottky diode is shown in the below figure. The vertical line in the below figure represents the current flow in the schottky diode and the horizontal line represents the voltage applied across the schottky diode.The V-I characteristics of schottky diode is almost similar to the P-N junction diode. However, the forward voltage drop of schottky diode is very low as compared to the P-N junction diode.

Applications of schottky diodes:

- Schottky diodes are used as general-purpose rectifiers.
- Schottky diodes are used in radio frequency (RF) applications.
- Schottky diodes are widely used in power supplies.
- Schottky diodes are used to detect signals.
- Schottky diodes are used in logic circuits.

UNIT- III

TRANSISTOR CHARACTERISTICS

BJT: Junction transistor, transistor current components, transistor equation, transistor configurations, transistor as an amplifier, characteristics of transistor in Common Base, Common Emitter and Common Collector configurations, Ebers-Moll model of a transistor, punch through/ reach through, Photo transistor, typical transistor junction voltage values.**FET:** FET types, construction, operation, characteristics, parameters, MOSFET-types, construction, operation, characteristics, comparison between JFET and MOSFET.

Transistors

- Unipolar Junction Transistor (UJT) ⇓ The current conduction is only due to one type of carriers ie majority carriers.
- Bipolar Junction Transistor (BJT) ⇓ The current conduction in bipolar transistor is due to both minority and majority carriers.

Bipolar Junction Transistor (BJT)

Construction :

* It's a 3 terminal device → Emitter (E), Base (B) & collector (c)
* Two Basic types
  - npn ⇓ 2 layers of n-type material sandwitching a Thin p-type layer is called npn Transistor
  - pnp ⇒ 2 layer of p-type material sandwitching a Thin n-type layer is called pnp Transistor.
* The Emitter terminal is heavily doped while the base & collector are lightly doped.
* The Thickness of the base layer is ~0.001 of that of the emitter (or) collector layer.

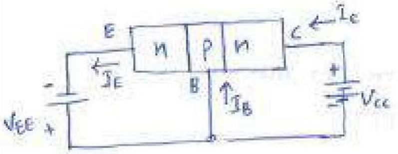
Symbols :

npn

pnp

Operations:

npn



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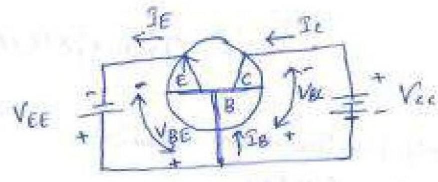
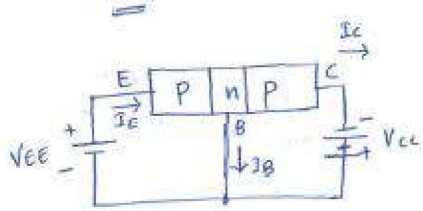


* The arrow at each Terminals points in the direction of conventional current.

* The current flow out of the E Terminal is referred as Emitter current, which is denoted as I_E.

* The current flow into the B terminal is referred as Base current, which is denoted as I_B & Collector terminal current is denoted as I_C.

pnp



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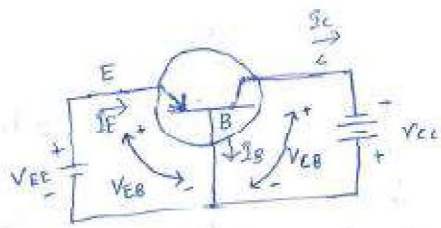


* The current flow into the E Terminal is referred as Emitter current which is denoted as I_E.

* The current flow out of the B & C terminals are referred as base & collector currents, which are denoted as I_B & I_C.

\# For current flow through the BJT its 2 PN Junctions (2 diodes back to back) must be properly biased.

\# One Junction is forward bias while the other is Reverse Bias.

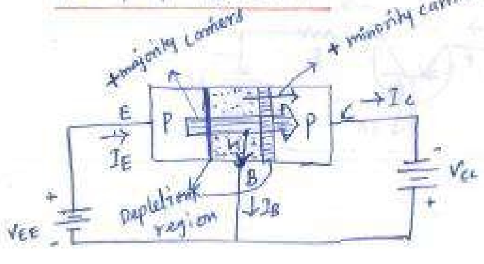
1. Forward Bias

   When the p side is applied +ve and n side is applied -ve in a Junction & applied voltage is greater than a Threshold 0.65V for Si

2. Reverse Bias

   When the p side is applied -ve and n side is applied +ve in a Junction & applied voltage is between 0 to a breakdown voltage.

For pnp Transistor



* The Emitter-Base Junction is forward biased While the collector-Base Junction is Reverse biased.

* The majority carriers will flow from E to B across forward bias junction.

* Because the Base layer is very thin & has a high resistance, most of these carriers will diffuse across the reverse bias junction into the collector in the same direction of the minority charges & only tiny amount of current will flow out of the Base Terminal.

* Typically collector currents are of the order of mA While Base currents are μA.

* Applying Kirchhoff's current law:

$$I_E = I_c + I_B$$

* The collector current is comprised of 2 components → majority & minority carriers.

* The minority current component is called leakage current, I_{CO} (I_c with Emitter terminal open).

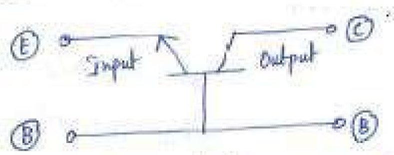
* So the collector current is

$$I_c = I_{c\,majority} + I_{CO\,minority}$$

Transistor Configurations:

1. Common Base (CB) configuration
2. Common Emitter (CE) configuration
3. Common collector (CC) configuration

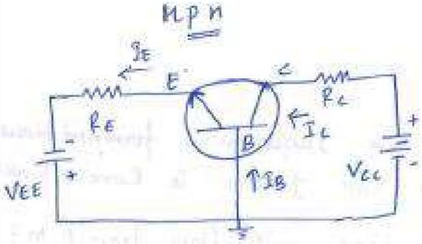
1. Common Base configuration



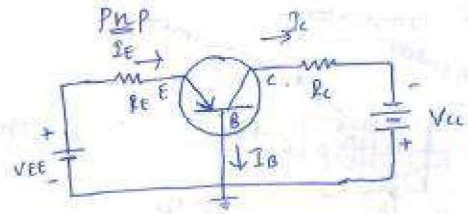
* The Base terminal is common to both i/p & o/p.

* The i/p is applied b/w the Emitter & the base & o/p is taken from collector & Base.

npn

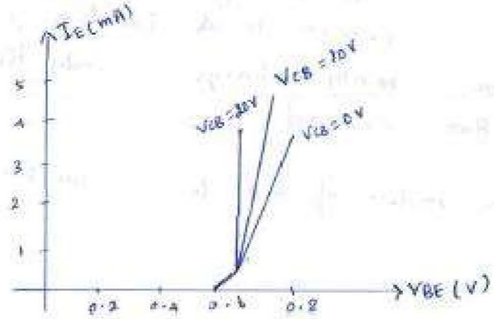


PNP



consider npn

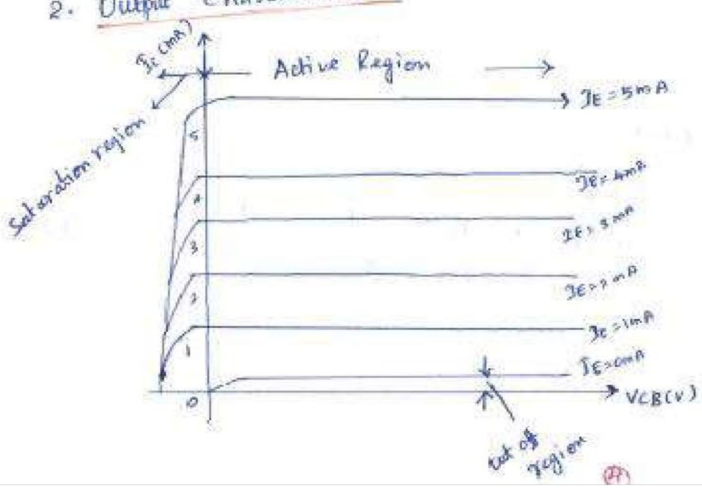
1. Input characteristics



* It shows the relation b/w input current I_E & input voltage V_{BE} for different value of output voltage V_{CB}.
* It resembles the characteristics of forward bias diode.

* I_E increase as V_{BE} increases for a fixed value of V_{CB}.
* As V_{CB} increases, the width of the depletion layer in the Base increases.
* The width of the Base available for conduction decreases.
* Hence, the width of the Base due to increase in Reverse bias
* The reduction in the width of the Base is known as Early Effect.
* Due to Early effect, the chance of recombination of electrons with holes in the Base decreases.
* As V_{CB} further increases, at one stage the depletion region completely Occupies the Base at which the collector-Base junction breaks down.
* This phenomenon is known as punch-through.

2. Output characteristics



* It shows the relationship b/w the o/p voltage V_{CB} & o/p current I_C for different values of input current I_E.

i) Cut-off Region

* Both the junctions are reverse biased.

* When the emitter-base junction is reverse biased, the current due to majority carrier ie I_E is zero.

* When the collector-base junction is reverse biased, the current due to minority carriers flows from the collector to the base is represented as I_{CBO}.

ii) Active Region

* The Emitter-base junction is forward biased & the collector-base junction is reverse biased.

* Once the V_{CB} reaches a value large enough to ensure a large portion of electrons enter the collector, I_C remains constant as shown by horizontal lines.

* As I_E increases, I_C increases.

iii) Saturation Region

* Both junctions are forward biased.

* When V_{CB} is -ve, the collector-base junction is actually forward biased

* Thus, graphs are drawn on the -ve side of V_{CB}.

Current Amplification factor (α)

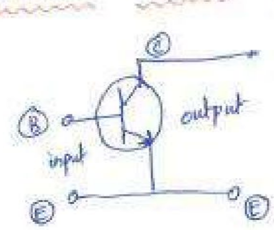
* It's the ratio of change in collector current to the change in Emitter current at constant collector-base voltage V_{CB}.

$$\alpha_{AC} = \frac{\Delta I_C}{\Delta I_E} \Big|_{V_{CB} = \text{constant}}$$

* If only DC values are considered

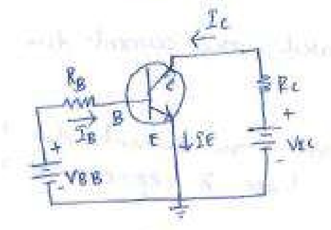
$$\alpha_{DC} = \frac{I_C}{I_E}$$

2. Common-Emitter configuration

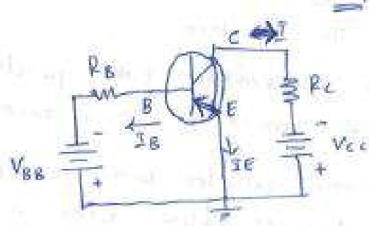


* Input is applied b/w base & Emitter and output is taken b/w collector & the emitter.

npn

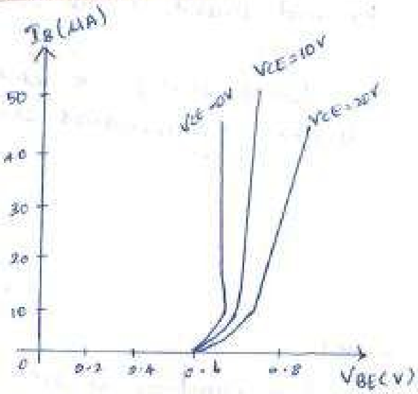


pnp



Consider npn

1. Input characteristics



* It shows the relationship b/w the i/p current I_B & i/p voltage VBE for different values of o/p voltage V_{CE}.

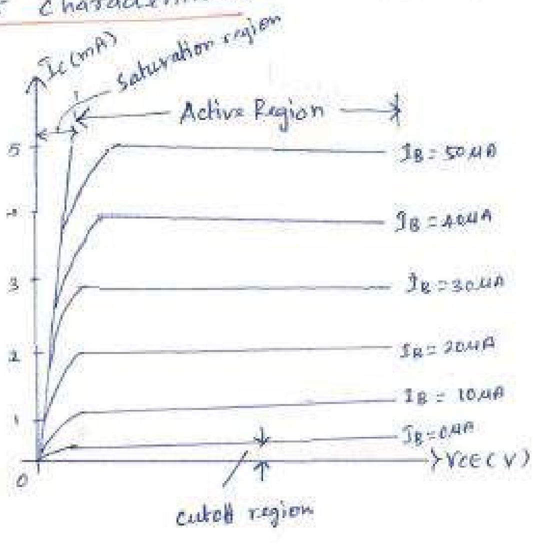
* It resembles the characteristics of forward bias diode.

* I/P current I_B increases as i/p volta VBE increases for fixed value of V_{CE}.

* As V_{CE} increases, the depletion region in the collector base increases which decreases the width of the base available for conduction.

* Hence I_B decreases due to early Effect & the graph shifts towards the x-axis.

2. Output characteristics



* It shows the relation b/w o/p current I_C & o/p voltage V_{CE} for different values of i/p current I_B.

i) Cut-off Region

* Both the junctions are reverse biased.
* When the emitter-base junction is reverse biased, the current due to majority carriers ie I_B is zero.
* When the collector-base junction is reverse biased. The current due to minority carriers flows from the collector to emitter which is represented as I_{CEO}.

ii) Active Region

* The Emitter-base junction is forward biased & the collector-base junction is reverse biased.
* As I_B is maintained constant, current I_C increases as reverse-biased voltage V_{CE} increases.

iii) Saturation Region

* Both junctions are forward biased.
* When V_{CE} is reduced to a small value such as 0.2 V, the collector base junction is actually forward biased.
* In this region, there is a large change in I_C with small change in V_{CE}

Current Amplification factor (β)

* It's defined as the change in collector current to the change in base current at constant collector-Emitter voltage V_{CE}.

$$\beta_{AC} = \frac{\Delta I_C}{\Delta I_B} \Big|_{V_{CE} = \text{constant}}$$

* If only DC values are considered

$$\beta_{DC} = \frac{I_C}{I_B}$$

Relation between α and β

$$I_E = I_C + I_B \quad —①$$

Also,

$$\beta_{DC} = \frac{I_C}{I_B} \quad —②$$

From ① $I_B = I_E - I_C$ —③

sub ③ in ② $\beta_{DC} = \dfrac{I_C}{I_E - I_C}$ —④

* Divide eqn ④ by I_E both Numerator & Denominator

$$④ \Rightarrow \beta_{DC} = \frac{I_C / I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} = \frac{I_C / I_E}{1 - \frac{I_C}{I_E}} \quad — ⑤$$

W.K.T $\alpha_{DC} = \frac{I_C}{I_E}$

Sub α_{DC} in eqn ⑤

$$⑤ \Rightarrow \beta_{DC} = \frac{\alpha_{DC}}{1 - \alpha_{DC}}$$

* If subscript DC is ignored

$$\beta = \frac{\alpha}{1-\alpha}$$

Collector Current (I_C):

* Apply KCL to the transistor

$$I_E = I_B + I_C \quad — Ⓐ$$

* The collector current has 2 components

$$I_C = I_{C\,majority} + I_{C\,minority}$$

$$I_C = \alpha I_E + I_{CO} \quad — Ⓑ$$

* For general purpose Transistors → I_C is measured in mA & I_{CO} is measured in μA (or) nA.

sub eq Ⓐ in Ⓑ

$$I_C = \alpha(I_B + I_C) + I_{CO}$$

$$= \alpha I_B + \alpha I_C + I_{CO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CO}$$

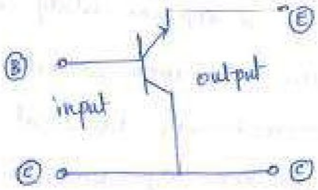
$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO} \qquad \because \beta = \frac{\alpha}{1-\alpha}$$

$$= \beta I_B + \frac{1}{1-\alpha} I_{CO}$$

sub $\frac{1}{1-\alpha} = (\beta+1)$ so we get

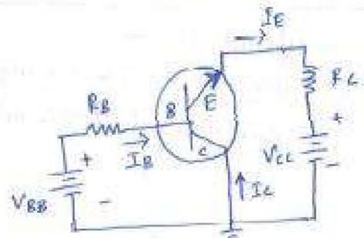
$$I_C = \beta I_B + (\beta+1) I_{CO}$$

3. Common-Collector Configuration

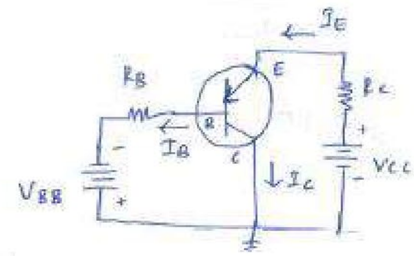


* The i/p is applied b/w base & collector & o/p is taken b/w Emitter & collector.

npn



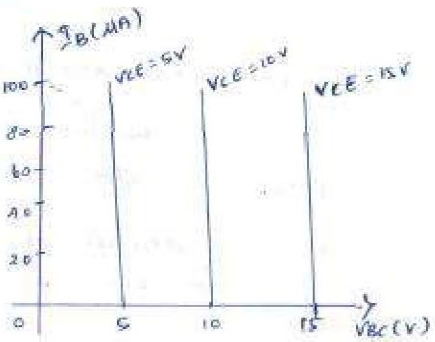
pnp



Consider npn

1) Input characteristics

* It shows the relation b/w i/p current I_B & i/p voltage V_{BC} for different values of o/p voltage V_{CE}.
* The i/p voltage V_{BC} is largely determined by the o/p voltage V_{CE}.



* The i/p current I_B decreases to 0 as i/p voltage V_{CB} increases slightly for fixed values of V_{CE}.

$$V_{CE} = V_{BE} + V_{BC}$$

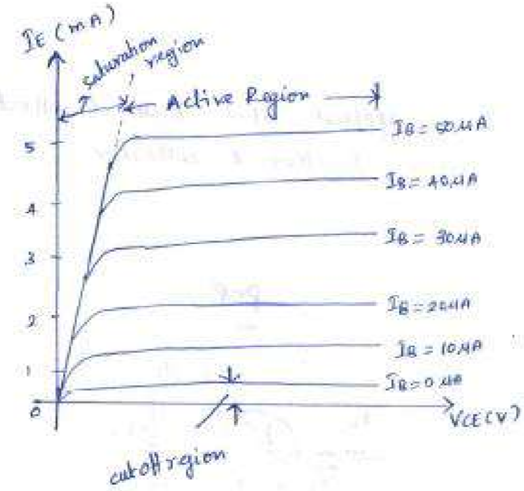
$$V_{BE} = V_{CE} - V_{BC}$$

* When V_{BC} is increased by keeping V_{CE} constant, V_{BE} decreases whic decreases I_B.

* ∴ If the value of V_{BE} is allowed to increase to a point where it's near to the value of V_{CE}, the value of V_{BE} approaches 0 & no base current will flow.

2) Output characteristics.

* It shows the relation b/w o/p current I_E & o/p voltage V_{CE} for different values of i/p current I_B.



* Since I_C is approximately equal to I_E, the common collector characteristics are identical to the common emitter o/p characteristics.

<u>Current Amplification factor (γ)</u>

* It's defined as the ratio of change in Emitter current to the change in base current at constant collector-emitter voltage V_{CE}.

$$\gamma_{AC} = \frac{\Delta I_E}{\Delta I_B} \Big|_{V_{CE} = \text{constant}}$$

* If only DC values are considered

$$\gamma_{DC} = \frac{I_E}{I_B}$$

Current components in a transistor:

The figure below shows the various current components which flow across the forward-biased emitter junction and reverse-biased collector junction in P-N-P transistor.

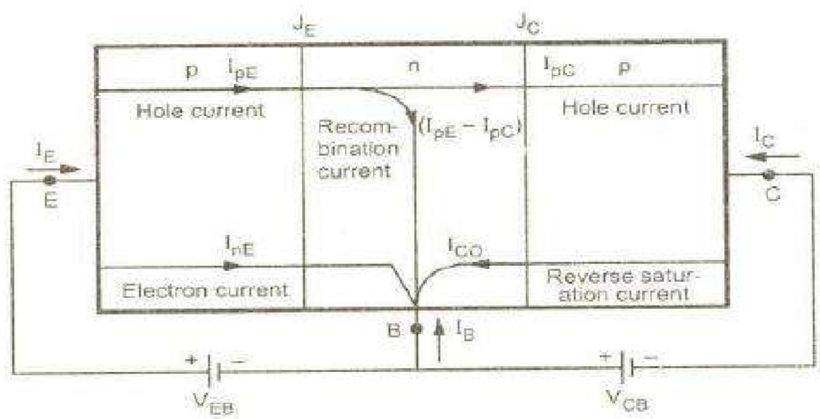


Figure. Current components in a transistor with forward-biased emitter and reverse-biased collector junctions.

The emitter current consists of the following two parts:

3. Hole current I_{pE} constituted by holes (holes crossing from emitter into base).
4. Electron current I_{nE} constituted by electrons (electrons crossing from base into the emitter).

Therefore, Total emitter current $I_E = I_{pE}$ (majority) + I_{nE} (Minority)

The holes crossing the emitter base junction J_E and reaching the collector base junction J_C constitutes collector current I_{pC}.

Not all the holes crossing the emitter base junction J_E reach collector base junction J_C because some of them combine with the electrons in the n-type base.

Since base width is very small, most of the holes cross the collector base junction J_C and very few recombine, constituting the base current $(I_{pE} - I_{pC})$.

When the emitter is open-circuited, I_E=0, and hence I_{pC}=0. Under this condition, the base and collector together current I_C equals the reverse saturation current I_{CO}, which consists of the following two parts: I_{PCO} caused by holes moving across J_C from N-region to P-region.

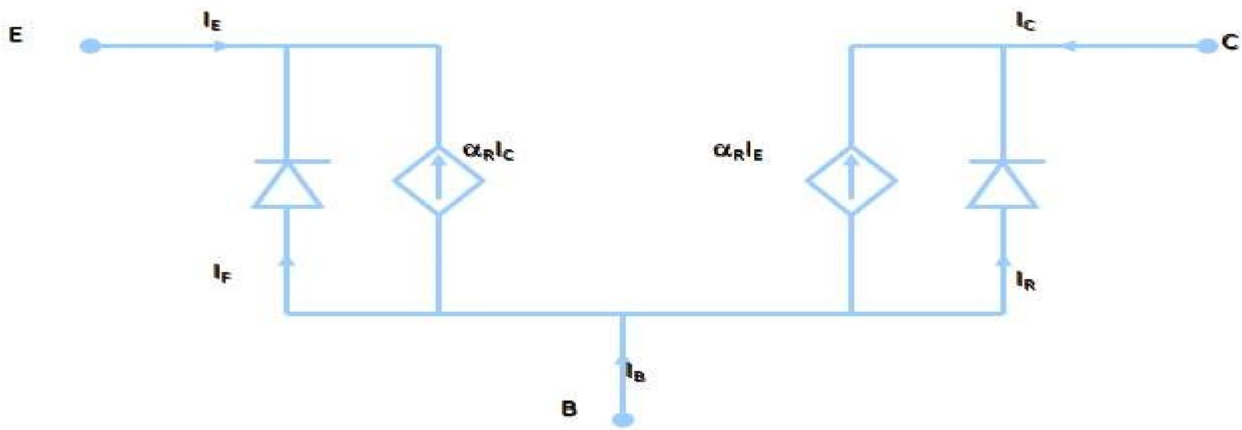
I_{nCO} caused by electrons moving across J_C from P-region to N-region. $I_{CO} = I_{nCO} + I_{pCO}$

In general, $I_C = I_{nC} + I_{pC}$

Thus for a P-N-P transistor, $\mathbf{I_E = I_B + I_C}$

Ebers-Moll model of a transistor:

The Eber-Moll Model for BJTs is fairly complex, but it is valid in all regions of BJT operation. The circuit diagram below shows all the components of the Eber-Moll Model:



α_R = Common-base current gain (in forward active mode)

α_F = Common-base current gain (in inverse active mode)

I_{ES} = Reverse-Saturation Current of B-E Junction

I_{CS} = Reverse-Saturation Current of B-C Junction

$I_C = \alpha_F I_F - I_R$

$I_B = I_E - I_C$

$I_E = I_F - \alpha_R I_R$

$I_F = I_{ES}$ [exp(qV_{BE}/kT)– 1] $I_R = I_C$ [exp (qV_{BC}/kT) – 1]

If I_{ES} & I_{CS} are not given, they can be determined using various BJT parameters.

Phototransistor:

A Phototransistor is an electronic switching and current amplification component which relies on exposure to light to operate. When light falls on the junction, reverse current flows which is proportional to the luminance. Phototransistors are used extensively to detect light pulses and convert them into digital electrical signals. These are operated by light rather than electric current. Providing large amount of gain, low cost and these phototransistors might be used in numerous applications.

It is capable of converting light energy into electric energy. Phototransistors work in a similar way to photo resistors commonly known as LDR (light dependant resistor) but are able to produce both current and voltage while photo resistors are only capable of producing current due to change in resistance. Phototransistors are transistors with the base terminal exposed. Instead of sending current into the base, the photons from striking light activate the transistor. This is because a phototransistor is made of a bipolar semiconductor and focuses the energy that is passed through it. These are activated by light particles and are used in virtually all electronic devices that depend on light in some way. All silicon photo sensors (phototransistors) respond to the entire visible radiation range as well as to infrared. In fact, all diodes, transistors, Darlington's, Triacs, etc. have the same basic radiation frequency response.

The structure of the phototransistor is specifically optimized for photo applications. Compared to a normal transistor, a photo transistor has a larger base and collector width and is made using diffusion or ion implantation.

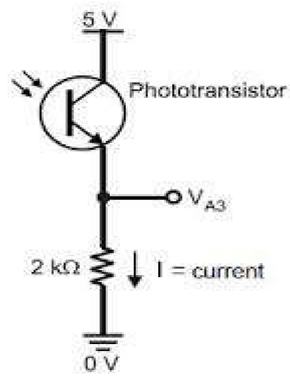


Figure 3.1: Phototransistor

Features:

- Low-cost visible and near-IR photo detection.
- Available with gains from 100 to over 1500.
- Moderately fast response times.
- Available in a wide range of packages including epoxy-coated, transfer-molded and surface mounting technology.
- Electrical characteristics similar to that of signal transistors.

A photo transistor is nothing but an ordinary bi-poplar transistor in which the base region is exposed to the illumination. It is available in both the P-N-P and N-P-N types having different configurations like common emitter, common collector and common base. Common emitter configuration is generally used. It can also work while base is made open. Compared to the conventional transistor it has more base and collector areas. Ancient photo transistors used single semiconductor materials like silicon and germanium but now a day's modern components uses materials like gallium and arsenide for high efficiency levels. The base is the lead responsible for activating the transistor. It is the gate controller device for the larger electrical supply. The collector is the positive lead and the larger electrical supply. The emitter is the negative lead and the outlet for the larger electrical supply.

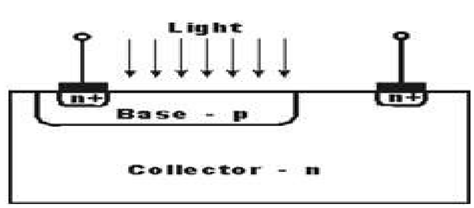


Figure 3.2: Construction of Phototransistor

With no light falling on the device there will be a small current flow due to thermally generated hole-electron pairs and the output voltage from the circuit will be slightly less than the supply value due to the voltage drop across the load resistor R. With light falling on the collector-base junction the current flow increases. With the base connection open circuit, the collector-base current must flow in the base-emitter circuit and hence the current flowing is amplified by normal transistor action. Collector base junction is very sensitive to light .Its working condition depends upon intensity of light. The base current from the incident photons is amplified by the gain of the transistor, resulting in current gains that range from hundreds to several thousands. A phototransistor is 50 to 100 times more sensitive than a photodiode with a lower level of noise.

A phototransistor works just like a normal transistor, where the base current is multiplied to give the collector current, except that in a phototransistor, the base current is controlled by the amount of visible or infrared light where the device only needs 2 pins.

FIELD EFFECT TRANSISTOR:

FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence the name Field Effect Transistor (FET). As current conduction is only by majority carriers, FET is said to be a unipolar device.

Based on the construction, the FET can be classified into two types as Junction FET (JFET) and Metal Oxide Semiconductor FET(MOSFET).

Depending upon the majority carriers, JFET has been classified into two types named as (1) N-channel JFET with electrons as the majority carriers and (2) P-channel JFET with holes as the majority carriers.

Construction of N-Channel JFET :

It consists of an N-type bar which is made of silicon. Ohmic contacts, (terminals) made at the two ends of the bar, are called Source and Drain.

Source (S) This terminal is connected to the negative pole of the battery. Electrons which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D) This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

Gate (G) Heavily doped P-type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together and called Gate G.

Channel The region BC of the N-type bar in the depletion region is called the channel. Majority carriers move from the source to drain when a potential difference V_{DS} is applied between the source and drain.

Operation of N-channel JFET:

When $V_{GS} = 0$ and $V_{DS} = 0$ When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions around the PN junction is uniform as shown in figure.

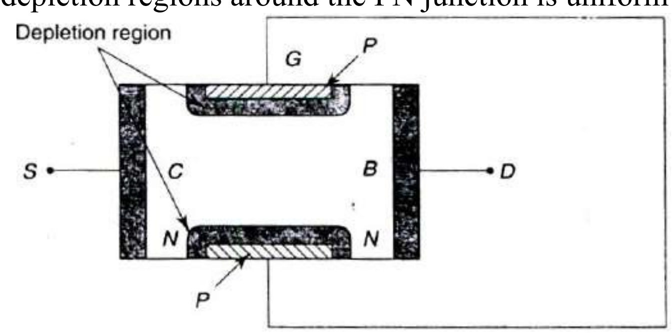


Figure 3.3: Construction of JFET

When $V_{DS} = 0$ and V_{GS} is decreased from zero. In this case PN junctions are reverse biased and hence the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased and hence the thickness of the depletion region in the channel increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cutoff. The value of V_{GS} which is required to cutoff the channel is called the cutoff voltage V_C.

When $V_{GS} = 0$ and V_{DS} is increased from zero. Drain is positive with respect to the source with $V_{GS} = 0$. Now the majority carriers (electrons) flow through the N-channel from source to drain. Therefore the conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:-

1. The number of the majority carriers (electrons) available in the channel, i.e. the conductivity of the channel.
2. The length *l* of the channel.
3. The cross sectional area *A* of the channel at *B*.
4. The magnitude of the applied voltage V_{DS}. Thus the channel acts as a resistor of resistance R given by

$$R = \frac{\rho l}{A} \qquad ....(1)$$

$$I_D = \frac{V_{DS}}{R} = \frac{A\,V_{DS}}{\rho l} \qquad ....(2)$$

where ρ is the resistivity of the channel. Because of the resistance of the channel and the applied voltage V_{DS}, there is a gradual increase of positive potential along the channel from source to drain. Thus the reverse voltage across the PN junctions increases and hence the thickness of the depletion regions also increases. Therefore the channel is wedge shaped, as shown in figure.

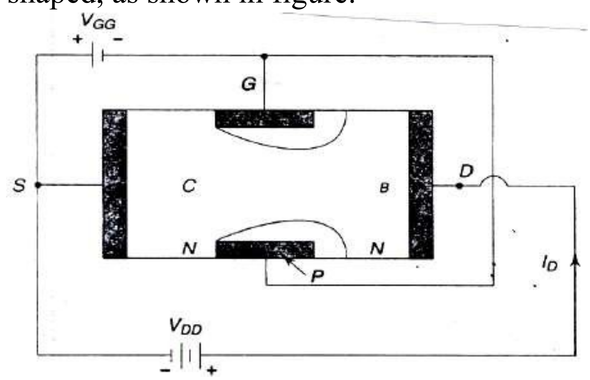


Figure 3.4: JFET under applied bias

As V_{DS} is increased, the cross-sectional area of the channel will be reduced. At a certain value V_P of V_{DS}, the cross-sectional area at B becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

As a result of the decreasing cross-section of the channel with the increase of V_{DS}, the following results are obtained.

(i) As V_{DS} is increased from zero, I_D increases along OP, and the rate of increase of I_D with V_{DS} decreases as shown in figure.

(ii) When $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off region increases. Hence there is no further increase of I_D.

(iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by BV_{DGO}. The variation of I_D with V_{DS} when $V_{GS} = 0$ is shown in figure by the curve OPBC.

When V_{GS} is negative and V_{DS} is increased. When the gate is maintained at a negative voltage less than the negative cutoff voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS} = 0$, but the values of V_P and BV_{DGO} are lower, as shown in figure.

From the curves, it is seen that above the pinch-off voltage, at a constant value of V_{DS}. I_D increases with an increase of V_{GS}. Hence a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

It can be seen from the curve that for the voltage $V_{DS} = V_P$, the drain current is not reduced to zero. If the drain current is to be reduced to zero, the ohmic voltage drop along the channel should also be reduced to zero. Further, the reverse biasing to the gate-source PN junction essential for pinching off the channel would also be absent.

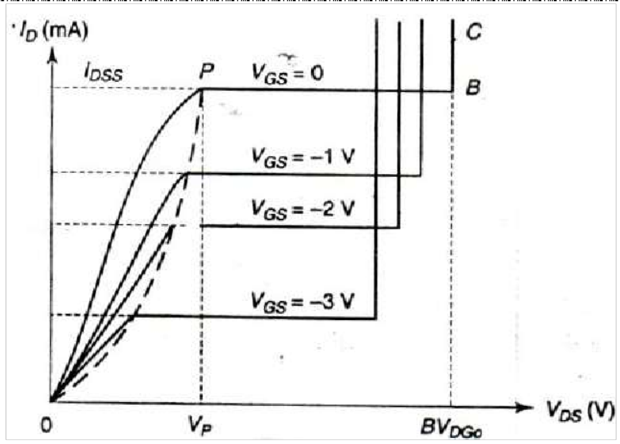


Figure 3.5: JFET Drain characteristics

The drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate; hence this device has been given the name "Field Effect Transistor".

In a bar of P-type semiconductor, the gate is formed due to N-type semiconductor. The working of the P-channel JFET will be similar to that of the N-channel JFET with proper alterations in the biasing circuits; in this case holes will be the current carriers instead of electrons. The circuit symbols for N-channel and P-channel JFETs are shown in figure. It should be noted that the direction of the arrow points in the direction of conventional current which would flow into the gate if the PN junction was forward biased.

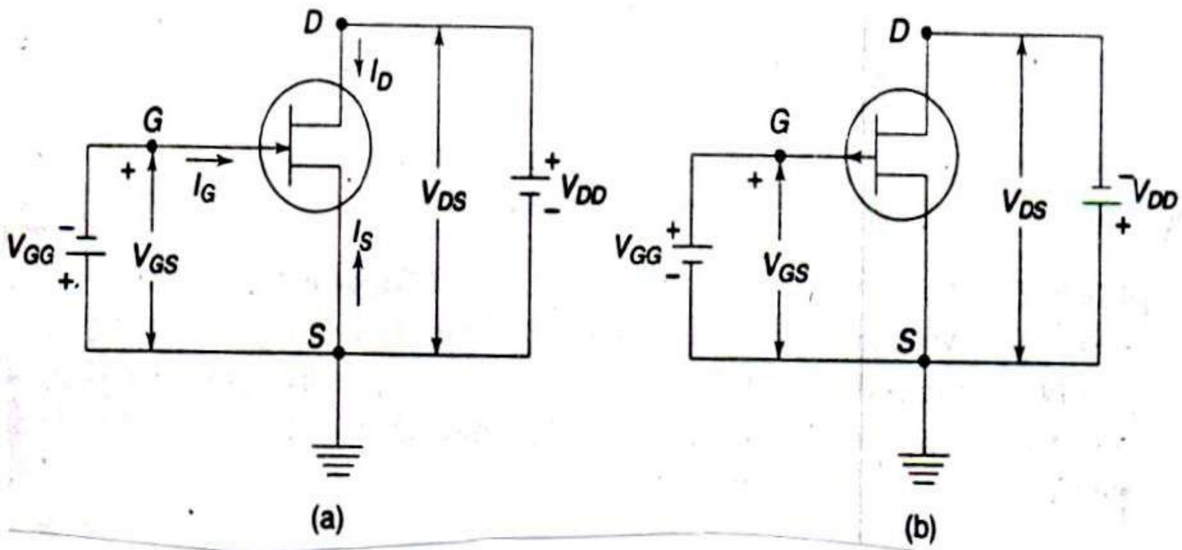


Figure 3.6: **Circuit Symbols for N and P Channel JFET**

MOSFET:

Metal Oxide Semiconductor Field Effect Transistor (MOSFET):

MOSFET is the common term for the Insulated Gate Field Effect Transistor (IGFET). There are two basic forms of MOSFET: (i) Enhancement MOSFET and (ii) Depletion MOSFET.

Principle:

By applying a transverse electric field across an insulator, deposited on the semiconducting material, the thickness and hence the resistance of a conducting channel of a semiconducting material can be controlled.

Enhancement MOSFET:

Construction: The construction of an N-channel Enhancement MOSFET is shown in figure. Two highly doped N^+ regions are diffused in a lightly doped substrate of P-type silicon substrate. One N^+ region is called the source S and the other one is called the drain D. They are separated by 1 mil (10^{-3} inch). A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layers, allowing contact with source and drain. Then a thin layer of metal aluminum is formed over the layer of SiO_2. This metal layer covers the entire channel region and it forms the gate G.

The metal area of the gate, in conjunction with the insulating oxide layer of SiO_2 and the semiconductor channel forms a parallel plate capacitor. This device is called the insulated gate FET because of the insulating layer of SiO_2. This layer gives an extremely high input resistance for the MOSFET.

Operation: If the substrate is grounded and a positive voltage is applied at the gate, the positive charge on G induces an equal negative charge on the substrate side between the source and drain regions. Thus an electric field is produced between the source and drain regions. The direction of the electric field is perpendicular to the plates of the capacitor through the oxide. The negative charge of electrons which are minority carriers in the P-type substrate forms an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semiconductor increases. Hence the conductivity increases and current flows from source to drain through the induced channel. Thus the drain current is enhanced by the positive gate voltage as shown in figure.

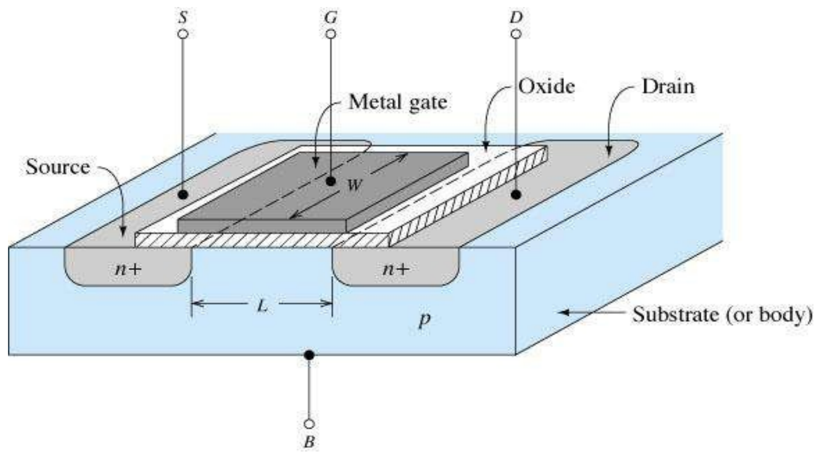


Figure 3.7: N – Channel Enhancement MOSFET

Depletion MOSFET :

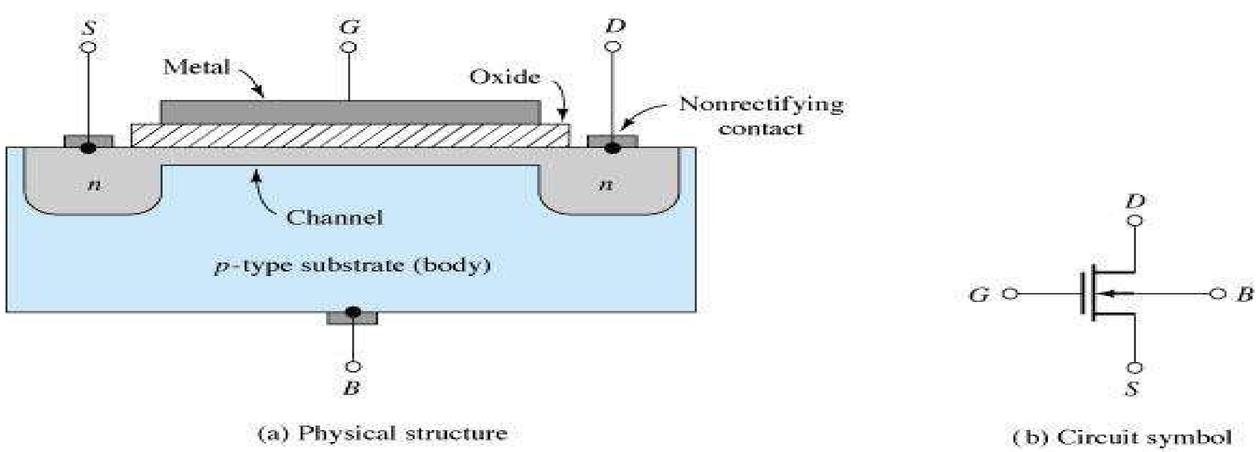


Figure 3.8: N-Channel Depletion MOSFET

The construction of an N-channel depletion MOSFET is shown in figure where an N-channel is diffused between the source and drain to the basic structure of MOSFET.

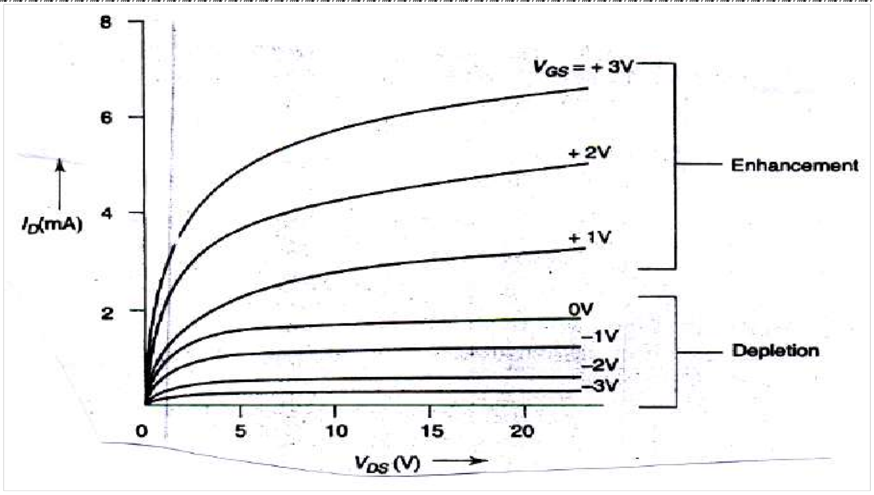


Figure 3.9: Volt-Ampere Characteristics of MOSFET

With $V_{GS} = 0$ and the drain D at a positive potential with respect to the source, the electrons (majority carriers) flow through the N-channel from S to D. Therefore the conventional current I_D flows through the channel D to S. If the gate voltage is made negative, positive charge consisting of holes is induced in the channel through SiO_2 of the gate-channel capacitor. The introduction of the positive charge causes depletion of mobile electrons in the channel. Thus a depletion region is produced in the channel. The shape of the depletion region depends on V_{GS} and V_{DS}. Hence the channel will be wedge shaped as shown in figure. When V_{DS} is increased, I_D increases and it becomes practically constant at a certain value of V_{DS}, called the pinch-off voltage. The drain current I_D almost gets saturated beyond the pinch-off voltage.

Since the current in an FET is due to majority carriers (electrons for an N-type material), the induced positive charges make the channel less conductive, and I_D drops as V_{GS} is made negative.

The depletion MOSFET may also be operated in an enhancement mode. It is only necessary to apply a positive gate voltage so that negative charges are induced into the N-type channel. Hence the conductivity of the channel increases and I_D increases. The volt-ampere characteristics are indicated in figure.

Comparison of JFET vs MOSFET:

JFETs and MOSFETs are quite similar in their operating principles and in their electrical characteristics. However, they differ in some aspects, as detailed below:

1. JFETs can only be operated in the **depletion mode** whereas MOSFETs can be operated in either depletion or in **enhancement mode**. In a JFET, if the gate is forward biased, excess- carrier injunction occurs and the gate current is substantial. Thus channel conductance is enhanced to some degree due to excess carriers but the device is never operated with gate forward biased because gate current is undesirable.
2. MOSFETs have input impedance much higher than that of JFETs. This is due to negligibly small leakage current.
3. JFETs have characteristic curves more flat than those of MOSFETs indicating a higher drain resistance.
4. When JFET is operated with a reverse bias on the junction, the gate current I_G is larger than it would be in a comparable MOSFET. The current caused by minority carrier extraction across a reverse-biased junction is greater, per unit area, than the leakage current that is supported by the oxide layer in a MOSFET. Thus MOSFET devices are more useful in electrometer applications than are the JFETs.

For the above reasons, and also because MOSFETs are somewhat easier to manufacture, they are more widely used than are the JFETs.

UJT (Unijunction Transistor):

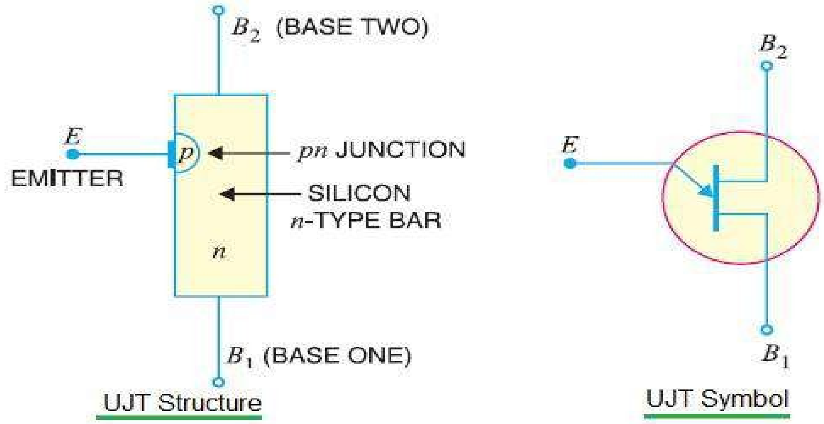


Figure 3.10.: Structure and Symbol of UJT

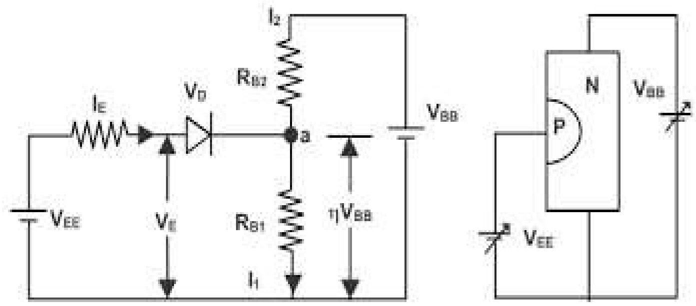


Figure 3.11.: Equivalent circuit of UJT

As shown it is n-type silicon bar with connections on both ends. The leads are referred as "B1" and "B2". Along the bar between the two bases , PN junction is constructed between P-type Emitter and N-type Bar. This lead is referred as "Emitter Lead-E". It is the short form of UnijunctionTransistor. t is 3 terminal switching device made of semiconductor materials. When UJT is triggered, I_E increases re-generatively until it is limited by V_E . Here I_E is emitter current and V_E is emitter power supply. Due to this feature, UJT is used in wide variety of applications such as sawtooth generator, pulse generator, switching etc. Device has only one PN junction and hence the term "UNI" in Unijunction Transistor (UJT). The UJT is also known as "Double Based Diode". This is due to the fact that it has only one PN junction. The two base terminals are derived from one single section of diode(or semiconductor material). In UJT, emitter part is heavily doped and n region is lightly doped. Hence resistance between two base terminals is quite high when emitter terminal is left open. The value of resistance is about 5 to 10 KOhm. UJT is a three terminal semiconductor switching device. As it has only one PN junction and three leads, it is commonly called as Unijunction Transistor.

The basic structure of UJT is shown in figure (a). It consists of a lightly doped silicon bar with a heavily-doped P-type material alloyed to its one side closer to B_2 for producing single PN junction. The circuit symbol of UJT is shown in figure (b).Here the emitter leg is drawn at an angle to the vertical and the arrow indicates the direction of the conventional current.

Characteristics of UJT:

Referring to figure (c), the interbase resistance between B_2 and B_1 of the silicon bar is $R_{BB} = R_{B1} + R_{B2}$. With emitter terminal open, if voltage V_{BB} is applied between the two bases, a voltage gradient is established along the N-type bar. The voltage drop across R_{B1} is given by $V_1 = \eta\ V_{BB}$ where the intrinsic stand-off ratio $\eta = R_{B1}/\ (R_{B1} + R_{B2})$. This voltage V_1 reverse biases the PN junction and emitter current is cut off. But a small leakage current flows from B_2 to emitter due to minority carriers. If a positive voltage V_E is applied to the emitter, the PN junction will remain reverse biased so long as V_E is less than V_1. If V_E exceeds V_1 by the cutin voltage V_r, the diode becomes forward biased. Under this condition, holes are injected into N-type bar. These holes are repelled by the terminal B_2 and are attracted by the terminal B_1. Accumulation of holes in E to B_1 region reduces the resistance in this section and hence emitter current I_E is increased and is limited by V_E. The device is now in the 'ON' state.

If a negative voltage is applied to the emitter, PN junction remains reverse biased and the emitter current is cut off. The device is now in the 'OFF' state.

As shown in figure, up to the peak point P, the diode is reverse biased. At P, the diode starts conducting and holes are injected into the N-layer. Hence resistance decreases thereby decreasing V_E for the increase in I_E. So there is a negative resistance region from peak point P to valley point V. After the valley point, the device is driven into saturation and behaves like a conventional forward biased PN junction diode.

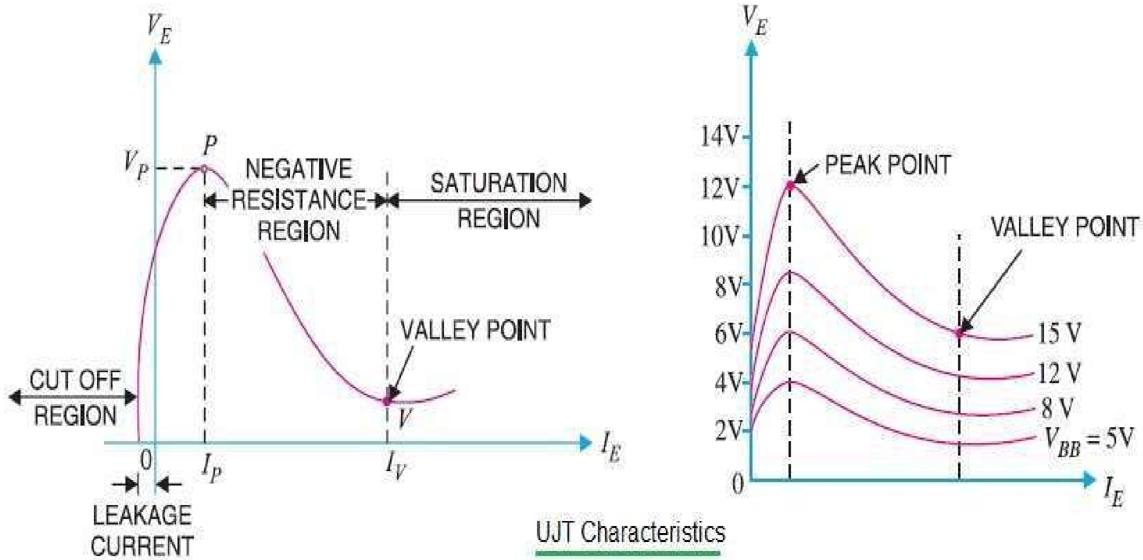


Figure 3.12: Characteristics of UJT

A unique characteristics of UJT is, when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply. Due to this negative resistance property, UJT can be employed in a variety of applications, viz. sawtooth wave generator, pulse generator, switching, timing and phase control circuits.

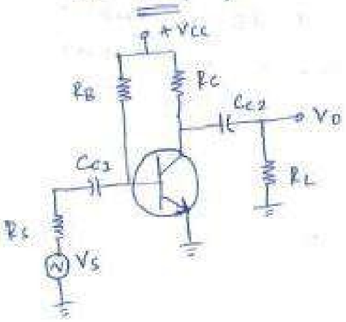
UNIT- IV

Transistor Biasing and Thermal Stabilization

Need for biasing, operating point, load line analysis, BJT biasing- methods, basic stability, fixed bias, collector to base bias, self bias, Stabilization against variations in V_{BE}, Ic, and β, Stability factors, (S, S', S''), Bias compensation, Thermal runaway, Thermal stability.
FET Biasing- methods and stabilization.

Load Line Analysis

CE Amplifier



* The basic function of a transistor is to do amplification.
* The weak signal is given to the transistor & amplified output is obtained from the collector.
* The process of raising the strength of weak signal without any change in its general shape is known as Amplification.
* A Transistor must be properly biased to operate as an amplifier.

* In CE amplifier the Capacitor C_{c1} is a DC blocking capacitor & couples AC input signal to the base of the Transistor.
* the capacitor C_{c2} is used to couple AC output of the amplifier to load R_L

DC Analysis:

For DC, $f = 0$

$$X_c = \frac{1}{2\pi f c} = \frac{1}{0} = \infty$$

* The DC equivalent circuit is obtained by replacing all capacitors by open circuit.

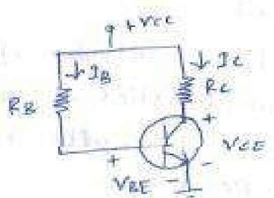


Fig: DC Equivalent circuit

Load Line:

* Applying KVL to the collector - Emitter circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CC} - V_{CE} = I_C R_C$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad \text{--- (1)}$$

* The eqn (1) represent the DC load line with slope is $-\frac{1}{R_C}$ & 'Y' intercept of $\frac{V_{CC}}{R_C}$.

* When $I_C = 0$ i.e. the transistor is in cutoff region

$$(1) \Rightarrow \quad 0 = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$$

$$\frac{V_{CE}}{\cancel{R_C}} = \frac{V_{CC}}{\cancel{R_C}}$$

$$V_{CE} = V_{CC}$$

* When $V_{CE} = 0$ i.e. the transistor is in saturation region

$$(1) \Rightarrow \quad I_C = -\frac{1}{R_C}(0) + \frac{V_{CC}}{R_C}$$

$$I_C = \frac{V_{CC}}{R_C}$$

* The two endpoints are $(V_{CC}, 0)$ & $\left(0, \frac{V_{CC}}{R_C}\right)$.

* A line passing through these points is called DC load line as the slope of this line depends on the DC load R_C.

Quiescent point

* Applying KVL to the base-Emitter circuit

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B R_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

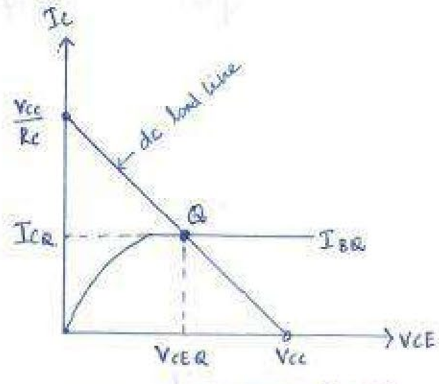


Fig: Load line and Q point

* This equation gives the value of base current.
* For this value of base current, o/p characteristics of the amplifier is plotted which intersects the DC load line at Q-point.
* Hence, Q point indicates quiescent (inactive, still) value of collector-Emitter voltage V_{CE} & collector current I_C.

Need for Biasing

* The Transistor can be operated in 3 regions: cutoff, active & saturation by applying proper biasing conditions

Region of operation	Emitter-Base Junction	collector-Base Junction
cutoff	Reverse biased	Reverse biased
Active	forward biased	Reverse biased
Saturation	forward biased	Forward biased

* In order to operate Transistor in the desired region we have to apply external dc voltage of correct polarity & magnitude to the 2 junctions of the Transistor. This is called biasing of the Transistor.
* Dc biasing is used to establish proper values of I_C & V_{CE} called the Dc operating point (or) quiescent point (or) Q point.
* The value of I_C & V_{CE} is expressed interms of operating point (or) Q point.
* For faithful amplification, Q point must be selected properly.
* The fulfilment of the below condition is known as transistor biasing

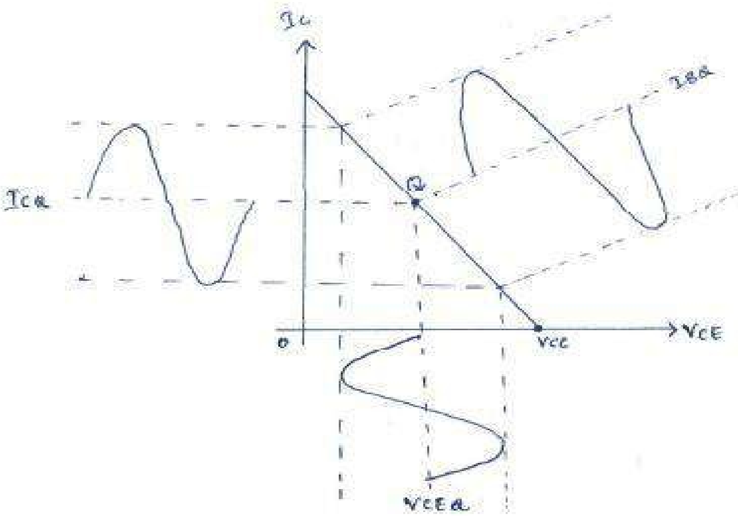
1. proper zero signal collector current I_C
2. proper base-emitter voltage V_{BE}
3. proper collector-emitter voltage V_{CE}

Selection of operating point:

* While fixing the Q-point it has to be seen that the o/p of the amplifier is a proper sinusoidal waveform for sinusoidal input without distortion.

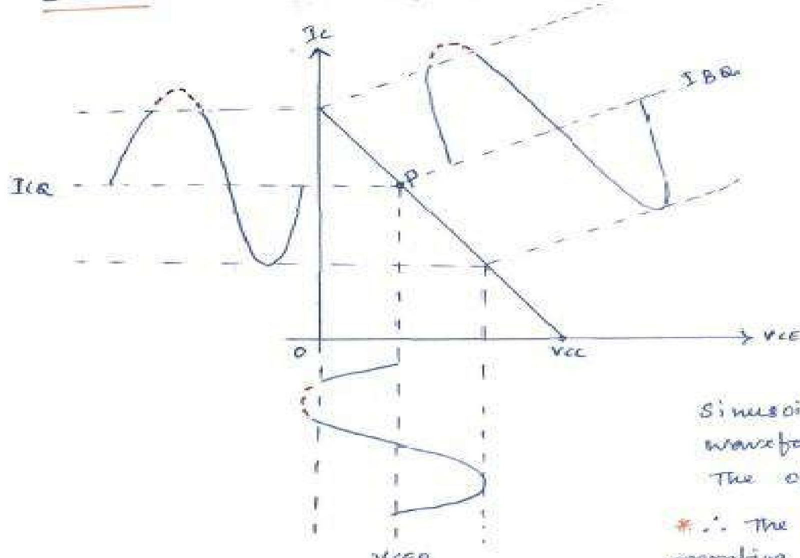
* If an amplifier is not biased properly, it can go into saturation (or) cutoff when an i/p signal is applied.
* By fixing the Q-point at different positions, we can observe the variation in I_C & V_{CE} corresponding to a given variation of I_B.

Case 1: When the Q point is located in the middle of the DC load line (or) center of the Active region



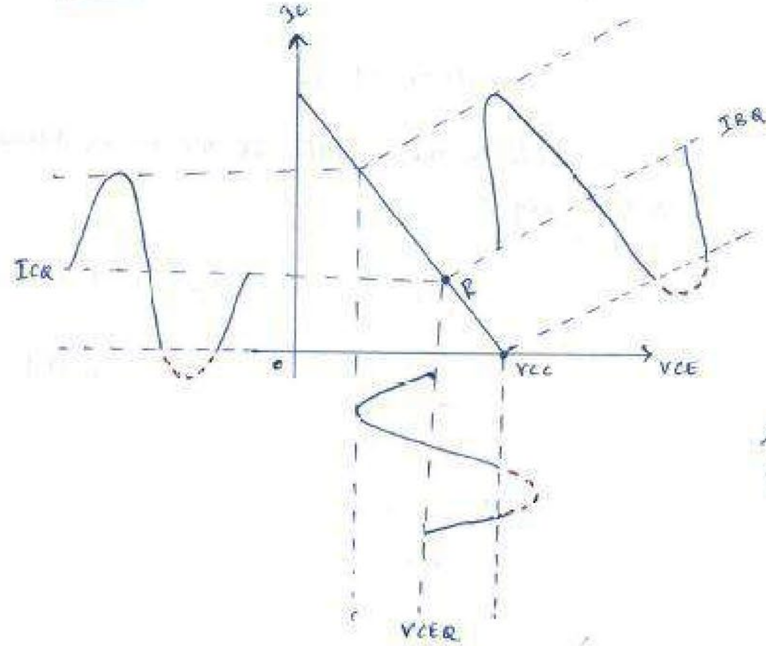
* The Q point is fixed at point Q.
* The o/p signal is sinusoidal waveform without any distortion
* Thus the point Q is the best operating point.

Case 2: When the Q point is located near the saturation region.



* The Q point is fixed at point P.
* The point P is very near to saturation region.
* The collector current I_C is clipped only at the positive half cycle.
* Eventhough the I_B varies sinusoidally, I_C is not a sinusoidal waveform i.e distortion is present at the o/p.
* ∴ The point P is not a suitable operating point.

Case 3: When the Q-point is located near the cut-off region



* The Q point is fixed at point R.
* The point R is very near to the cut off region.
* The Ic is clipped at the negative half cycle.
* So point R is also not a suitable Q point (or) operating point.

Variation of Q-point (or) Factors Affecting stability of Q-point

* The biasing circuit should be designed to fix the operating point (or Q-point at the centre of the active region.
* But only fixing of the operating point is not sufficent.
* While designing the biasing circuit, care should be taken so that the Q-point will not shift into an underirable region (ie cutoff or saturat
* Designing the bias circuit to stabilize the Q-point is taken as bias stability.

Temperature

1) I_{CO}

* The flow of current in the circuit produces heat at the junctions.
* This heat increases the temperature at the junctions.
* We know that the minority carriers are temperature dependent
* They increase with Temperature.
* The increase in the minority carriers increases the leakage curre I_{CBO}.

$$\because \; I_{CEO} = (1+\beta) I_{CBO}$$

* I_{CBO} doubles for every 10°C rise in temperature.

* Increase in I_{CEO} in turn Increase in the collector current.

$$\therefore I_C = \beta I_B + I_{CEO}$$

* The increase in I_C further raises the temperature at the collector junction & the same cycle repeats.

* The excessive increase in I_C shifts the Q-point into the saturation region, changing the operating condition set by biasing circuit.

* The power dissipation at collector base junction is

$$P_D = V_C I_C$$

* The increase in the I_C increases the power dissipated at the collector junction.

* This in turn further increase the temperature of the junction & hence increase the I_C.

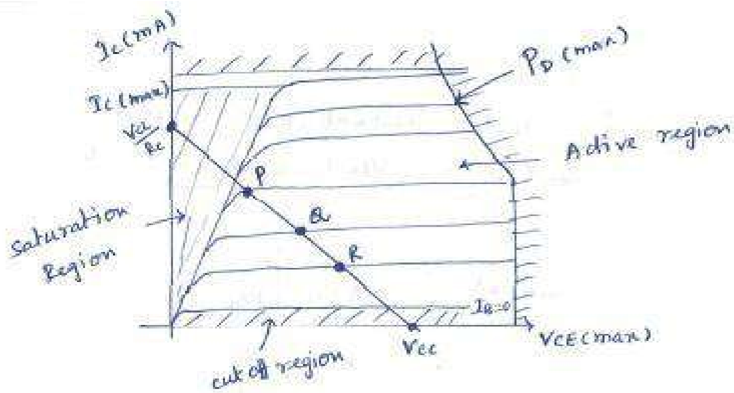
* The power is cumulative.

* The excess heat produced at the collector base junction may even burn & destroy the transistor.

* This situation is called Thermal runaway of the transistor.

* For any Transistor the maximum power dissipation is always a fixed value.

* This known as maximum power dissipation rating of a Transistor.



* The hyperbola give The maximum power dissipation for Transistor

* If This limit is crossed The device will fail.

2) V_{BE}

* V_{BE} changes with temperature at the rate of 2.5 mV/°C

* I_B depends upon V_{BE}

* I_B depends on V_{BE} & I_C depends on I_B, I_C depends on V_{BE}.

* $\therefore I_C$ changes with temperature due to changes in V_{BE}

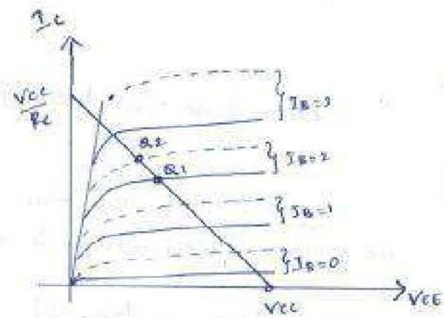
* The change in I_C changes the Q-point.

3) β_{dc}

* It's also temperature dependent.
* As β_{dc} varies, I_c also varies, since $I_c = \beta I_B$
* The change in I_c change the Q-point.

Transistor current gain $h_{FE} | \beta$

* There are changes in the Transistor parameters among different units of the same type, same number.
* If we take 2 transistor units of same type & use them in the circuit, there is change in the β value in actual practice.
* The biasing circuit is designed according to the required β value.
* But due to change in β from unit to unit, the Q-point may shift.



* This fig: shows the CE o/p characteristics for 2 Transistor of the same type.
* The dashed characteristics are for a Transistor whose β is much larger than that of the Transistor represent by solid curves.

Stability Factors

S :

* The rate of change of collector current (I_c) with respect to collector leakage current (I_{co}) at constant V_{BE} & β is called stability factor.

$$S = \frac{\partial I_c}{\partial I_{co}}\Big|_{V_{BE} \,\&\, \beta \text{ constant}} = \frac{\Delta I_c}{\Delta I_{co}}\Big|_{V_{BE} \,\&\, \beta \text{ constant}}$$

$$= \frac{\Delta I_{c2} - \Delta I_{c1}}{\Delta I_{co2} - \Delta I_{co1}}\Big|_{V_{BE} \,\&\, \beta \text{ constant}}$$

S' :

* The rate of change of collector current (I_c) with respect to V_{BE} at constant I_{co} & β is called stability factor S'.

$$S' = \frac{\partial I_c}{\partial V_{BE}}\Big|_{I_{co} \,\&\, \beta \text{ constant}} = \frac{\Delta I_c}{\Delta V_{BE}}\Big|_{I_{co} \,\&\, \beta \text{ constant}} = \frac{\Delta I_{c2} - \Delta I_{c1}}{\Delta V_{BE_2} - \Delta V_{BE_1}}\Big|_{I_{co} \,\&\, \beta \text{ constant}}$$

S'':

* The rate of change of collector current (I_C) with respect to β at constant I_{CO} & V_{BE} is called stability factor S''.

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO}\ \&\ V_{BE}\ \text{constant}} = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO}\ \&\ V_{BE}\ \text{constant}}$$

$$= \left.\frac{\Delta I_{C2} - \Delta I_{C1}}{\Delta \beta_2 - \Delta \beta_1}\right|_{I_{CO}\ \&\ V_{BE}\ \text{constant}}$$

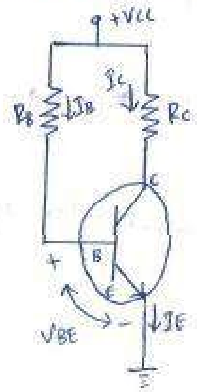
* The total change in collector current over a specified temperature range is obtained by expressing this change as the sum of individual changes due to 3 stability factors.

$$\Delta I_C = S \Delta I_{CO} + S' \Delta V_{BE} + S'' \Delta \beta$$

Different types of Biasing circuits / various biasing Methods for BJT

1. Fixed Bias
2. collector to Base Bias / Biasing with Feedback Resistor
3. Self Bias (or) Voltage Divider Bias

1. Fixed Bias / Base Bias



Dc Analysis:

* For Dc $f = 0$

$$X_C = \frac{1}{2\pi f c} = \frac{1}{0} = \infty$$

collector current (I_C):

* Apply KVL to the Base - Emitter circuit

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

* When V_{CC} & R_B are selected for a circuit I_B is fixed. Hence, the circuit is called Fixed bias circuit.

$$I_C = \beta I_B = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)$$

Collector Emitter Voltage (V_{CE})

* Apply KVL to the collector - Emitter circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

Load line Analysis

* Apply KVL to the collector- Emitter circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C R_C = -V_{CE} + V_{CC}$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$$

* This eqn represents dc load line with slope of $-\frac{1}{R_C}$ & y-intercept of $\frac{V_{CC}}{R_C}$.

* When $I_C = 0$ i.e The transistor is in cutoff region

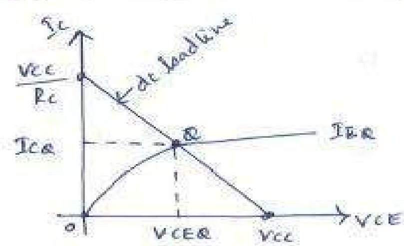
$$V_{CE} = V_{CC}$$

* When $V_{CE} = 0$ i.e the transistor is in saturation region

$$I_C = \frac{V_{CC}}{R_C}$$

* Thus the 2 end points are $(\underset{\substack{\downarrow \\ (x) \\ \downarrow \\ V_{CE}}}{V_{CC}}, \underset{\substack{\downarrow \\ (y) \\ \downarrow \\ I_C}}{0})$ & $(\underset{\substack{\downarrow \\ x \\ \downarrow \\ V_{CE}}}{0}, \underset{\substack{\downarrow \\ y \\ \downarrow \\ I_C}}{\frac{V_{CC}}{R_C}})$

* By joining this 2 end points Dc load line is drawn.



* The saturation current for the circuit is $I_{C\,sat} = \frac{V_{CC}}{R_C}$.

Stability factors

S:

$$S = \frac{\partial I_C}{\partial I_{CO}}\bigg|_{V_{BE}\ \&\ \beta\ \text{constant}} \quad \text{(or)} \quad \frac{\Delta I_C}{\Delta I_{CO}}\bigg|_{V_{BE}\ \&\ \beta\ \text{constant}}$$

* We know that

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

* No collector current present in this equation. so $\frac{\partial I_B}{\partial I_C} = 0$ —(1)

* We know I_C

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

* differentiate I_C with respect to I_C we get

$$\frac{\partial I_C}{\partial I_C} = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CO}}{\partial I_C} \qquad \because \frac{\partial I_C}{\partial I_{CO}} = S$$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \times \frac{1}{S}$$

$$1 - \beta \frac{\partial I_B}{\partial I_C} = \frac{1+\beta}{S}$$

$$\boxed{S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}} \quad \text{--- ②}$$

* Substitute ① in ②

$$S = \frac{1+\beta}{1-\beta(0)}$$

$$\boxed{S = 1+\beta}$$

S':

$$S' = \frac{\partial I_C}{\partial V_{BE}} \bigg|_{I_{CO} \,\&\, \beta \text{ constant}} \text{ (or) } \frac{\Delta I_C}{\Delta V_{BE}} \bigg|_{I_{CO} \,\&\, \beta \text{ constant}}$$

* W.K.T

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

* substitute I_B in I_C

$$I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right) + (1+\beta) I_{CO}$$

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{CO} \quad \text{--- ③}$$

* differentiate w.r.to V_{BE}

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \beta/R_B + 0$$

$$\boxed{S' = -\frac{\beta}{R_B}}$$

Relation between S & S'

$$S = 1+\beta \qquad S' = \frac{-\beta}{R_B}$$

In S' Multiply numerator & denominator by $(1+\beta)$ we get

$$S' = \frac{-\beta(1+\beta)}{R_B(1+\beta)} = \frac{-\beta S}{R_B(1+\beta)} \qquad \because S = 1+\beta$$

S'':

$$S'' = \frac{\partial I_C}{\partial \beta}\Big|_{V_{BE}\ \&\ I_{CO}\ \text{constant}} = \frac{\Delta I_C}{\Delta \beta}\Big|_{V_{BE}\ \&\ I_{CO}\ \text{Constant}}$$

From (3)

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{CO}$$

differentiate w.r.to 'β'

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B} + I_{CO}$$

$$\because I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= I_B + I_{CO}$$

$$= I_B + 0 \qquad \because I_B \gg I_{CO}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta} \qquad \because I_B = \frac{I_C}{\beta}$$

$$\boxed{S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta}}$$

Relation b/w S & S''

$$S = 1+\beta \qquad S'' = \frac{I_C}{\beta}$$

In S'' Multiply Numerator & denominator by $(1+\beta)$ we get

$$S'' = \frac{I_C(1+\beta)}{\beta(1+\beta)} = \frac{I_C S}{\beta(1+\beta)} \qquad \because S = 1+\beta$$

Advantages:

* Simple circuit which uses very few components.
* The operating point can be fixed anywhere in the active region of the characteristics by simply changing the value of R_B. Thus it provides maximum flexibility in the design.

Disadvantages

1. Thermal stability is not provided by this circuit. So the operating point is not maintained.

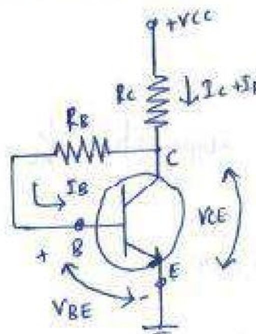
$$I_C = \beta I_B + I_{CEO}$$

2. Since $I_C = \beta I_B$ & I_B is already fixed; I_C depends on β which changes unit to unit & shifts the operating point.

The stabilization of operating point is very poor in the fixed bias circuit. Because of this reason the fixed bias circuit need some modifications.

In the modified circuit, R_B is connected b/w collector & base. Hence the circuit is called collector to base bias circuit.

2. Collector to Base Bias | Biasing with Feedback Resistor



* It's an improvement over the fixed bias method
* The resistor is connected b/w the base & the collector of the transistor. Hence the circuit is called collector to base bias circuit.
* Thus I_B flows through R_B & (I_C+I_B) flows through the R_C.

DC Analysis

* For DC $f=0$

$$X_C = \frac{1}{2\pi f C} = \frac{1}{0} = \infty$$

Collector Current I_C

* Apply KVL to the base-Emitter circuit

$$V_{CC} - (I_B+I_C)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - (\beta+1)I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_B((\beta+1)R_C + R_B) - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B((\beta+1)R_C + R_B)$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_C}}$$

* If there is a change in β due to piece to piece variation b/w transistors, then I_C tends to increase. As the result voltage drop across R_C increases.
* The supply voltage V_{CC} is constant, due to increase in $I_C R_C$, V_{CE} decreases. Due to reduction in V_{CE}, I_B decreases. This I_B reduction in lead to increase I_C.

W.K.T $I_B = \frac{I_C}{\beta} \Rightarrow I_C = \beta I_B$

$$I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_C} \right]$$

Collector Emitter Voltage V_{CE}

* Apply KVL to the collector - Emitter circuit

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$

Load Line Analysis

* Apply KVL to the collector - Emitter circuit

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

* Assume $I_B + I_C \simeq I_C$

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$$

* The equation represents a DC load line with slope of $-\frac{1}{R_C}$ & y-intercept $\frac{V_{CC}}{R_C}$.

* When $I_C = 0$ ie Transistor is in cut-off region

$$V_{CE} = V_{CC}$$

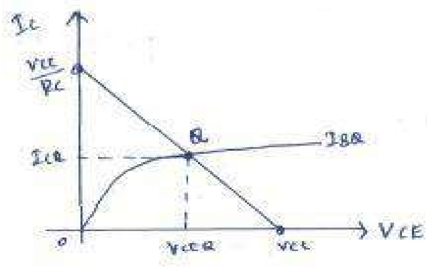
* When $V_{CE} = 0$ ie Transistor is in saturation region

$$I_C = \frac{V_{CC}}{R_C}$$

* Thus the 2 end points are $(V_{CC}, 0)$ & $(0, \frac{V_{CC}}{R_C})$. by joining the 2 end points DC load line is drawn.

* From Base - Emitter circuit

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_C}$$



The saturation current for the circuit is $I_{C\,sat} = \frac{V_{CC}}{R_C}$

Stability Factors

S:

* Apply KVL to the base - Emitter junction

$$V_{CC} = I_C R_C + I_B (R_C + R_B) + V_{BE}$$

* When I_B changes by ∂I_B & I_C changes by ∂I_C There is no effect on V_{CC} & V_{BE}

* So the equation becomes

$$0 = \partial I_C R_C + \partial I_B (R_C + R_B) + 0$$

$$\partial I_B (R_C + R_B) = -\partial I_C R_C$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B} \quad -①$$

* substitute ① in S

$$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{1+\beta}{1-\beta\left(\frac{-R_C}{R_C+R_B}\right)}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$$

* The collector - Base bias circuit is having Lesser stability factor Than fixed bias circuit.

* Hence the circuit provides better stability than fixed bias circuit

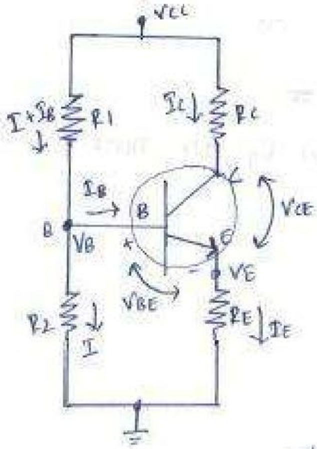
S':

$$S' = \frac{-\beta}{R_B + (1+\beta)R_C}$$

S'':

$$S'' = \frac{I_C}{\beta}\left(\frac{S}{1+\beta}\right)$$

3. Voltage Divider Bias / Self Bias / potential divider Bias



* The biasing is provided by R_1, R_2 & R_E.
* The resistors R_1 & R_2 act as a potential divider giving a fixed voltage to point B ie base.
* If I_C increases due to change in temperature (or β, the I_E also Increases & the voltage drop across R_E increases, decreasing the V_{BE}.
* Due to reduction in V_{BE}, I_B & I_C also reduced.
* Due to reduction in VBE, IB & IC also reduced.

* ∴ We can say that negative feedback exist in the Emitter bias circuit.

* The voltage across R_2 is the base voltage V_B.
* Apply voltage divider Theorem to find V_B we get

$$V_B = \frac{R_2(I)}{R_1(I+I_B)+R_2(I)} \times V_{CC}$$

$\because I >> I_B$ so we can omit I & I_B

So

$$V_B = \frac{R_2}{R_1+R_2} V_{CC}$$

* The voltage across R_E is V_E

$$V_E = I_E R_E = V_B - V_{BE}$$

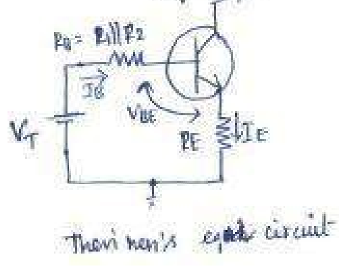
$$\therefore I_E = \frac{V_B - V_{BE}}{R_E}$$

* Apply KVL to the collector - Emitter circuit we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Modified circuit



Thevinen's eqvt circuit

* Here, R_1 & R_2 are replaced by R_B & V_T, where R_B is the parallel combination of R_1 & R_2 & V_T is the Thevenin's voltage.
* R_B is calculated as $R_B = \frac{R_1 R_2}{R_1+R_2}$

* Apply KVL to the Base - Emitter junction

$$V_T = I_B R_B + V_{BE} + I_E R_E \qquad \because I_E = I_C + I_B$$

$$= I_B R_B + V_{BE} + (I_C + I_B) R_E$$

$$= I_B R_B + V_{BE} + I_C R_E + I_B R_E$$

$$V_T = I_B (R_B + R_E) + V_{BE} + I_C R_E$$

$$V_{BE} = V_T - I_B (R_B + R_E) - I_C R_E$$

Stability Factors

$\underline{S}$

* Here the Thevinen's voltage V_T is given by

$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2} \qquad \text{\& } R_1 \text{ \& } R_2 \text{ replaced by } R_B.$$

* Apply KVL to the base - Emitter junction

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E \quad —①$$

* differentiate eqn ① w.r. to I_C & V_{BE} to be independent of I_C we get

$$0 = \frac{\partial I_B}{\partial I_C} R_B + 0 + \frac{\partial I_B}{\partial I_C} R_E + \frac{\partial I_C}{\partial I_C} R_E$$

$$0 = \frac{\partial I_B}{\partial I_C} (R_B + R_E) + R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E} \quad —②$$

* W.K.T

$$S = \frac{1+\beta}{1 - \beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{1+\beta}{1 - \beta\left(\frac{-R_E}{R_B + R_E}\right)} = \frac{1+\beta}{1 + \beta\left(\frac{R_E}{R_B + R_E}\right)}$$

* Take LCM

$$S = \frac{(1+\beta)(R_B + R_E)}{R_B + R_E + \beta R_E} = \frac{(1+\beta)(R_B + R_E)}{R_B + (1+\beta) R_E}$$

* Dividing each term by R_E we get

$$S = \frac{(1+\beta)\left(\frac{R_B}{R_E} + \frac{R_E}{R_E}\right)}{\frac{R_B}{R_E} + (1+\beta)\frac{R_E}{R_E}} = \frac{(1+\beta)\left(1 + \frac{R_B}{R_E}\right)}{(1+\beta) + \frac{R_B}{R_E}}$$

* The ratio R_B/R_E controls value of stability factor S.
* If $R_B/R_E << 1$ then $S = \frac{1+\beta}{1+\beta} = 1$

$\underline{S'}$

$$S' = \frac{\partial I_C}{\partial V_{BE}} \Big| I_{CO} \text{ \& } \beta \text{ constant}$$

* w.k.T

$$I_C = (1+\beta) I_{CO} + \beta I_B \quad — ①$$

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E \quad — ②$$

$$V_{BE} = V_T - (R_E + R_B) I_B - R_E I_C \quad — ③$$

* By rewriting the eqn ① interms of I_B

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta} \quad — ④$$

* substitute I_B in eqn ③ we get

$$③ \quad V_{BE} = V_T - (R_E + R_B) I_B - R_E I_C$$

$$= V_T - (R_E + R_B) \left[\frac{I_C - (1+\beta) I_{CO}}{\beta} \right] - R_E I_C$$

$$= V_T - \frac{(R_E + R_B) I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{CO}}{\beta} - R_E I_C$$

* Take the common term's Outside

$$V_{BE} = V_T - \frac{\left[(1+\beta) R_E + R_B \right] I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{CO}}{\beta} \quad — ⑤$$

* differentiate eqn ⑤ w.r.to V_{BE}

$$\underbrace{\frac{\partial V_{BE}}{\partial V_{BE}}}_{1} = 0 - \left(\frac{(1+\beta) R_E + R_B}{\beta} \right) \frac{\partial I_C}{\partial V_{BE}} + 0$$

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_E}$$

$$S' = \frac{-\beta}{R_B + (1+\beta) R_E}$$

$\underline{S'':}$

$$S'' = \frac{\partial I_C}{\partial \beta} \Big| I_{CO} \text{ \& } V_{BE} \text{ as constants}$$

$$V_{BE} = V_T - \frac{(R_B + (1+\beta)R_E)I_C}{\beta} + \underbrace{\left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right]I_{co}}_{V'}$$

$$= V_T - \frac{[R_B + (1+\beta)R_E]I_C}{\beta} + V' \quad \text{--- (6)}$$

* We can rewrite the eqn (6) interms of I_C

$$\frac{[R_B + (1+\beta)R_E]I_C}{\beta} = V_T - V' - V_{BE}$$

$$I_C = \frac{(V_T - V' - V_{BE})\beta}{R_B + (1+\beta)R_E} \quad \text{--- (7)} \Rightarrow \frac{u}{v} \text{ format}$$

$$\hookrightarrow \frac{v\,du - u\,dv}{v^2}$$

* differentiating eqn (7) w.r.to β

$$\frac{\partial I_C}{\partial \beta} = \frac{R_B + (1+\beta)R_E(V_T - V' - V_{BE}) - \beta(V_T - V' - V_{BE})R_E}{(R_B + (1+\beta)R_E)^2}$$

* Multiply numerator & denominator by $(1+\beta)$ & β

$$= \frac{(1+\beta)(R_B + R_E)\,(V_T - V' - V_{BE})\beta}{\beta(1+\beta)\underbrace{(R_B + R_E(1+\beta))}_{S}\underbrace{[R_B + R_E(1+\beta)]}_{I_C}}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{S}{\beta(1+\beta)} \times I_C$$

$$S'' = \frac{I_C\, S}{\beta(1+\beta)}$$

Advantages

* The stability factor S for voltage divider bias is less as compared to another biasing circuit

* So this circuit is more stable & hence it's most commonly used.

Load line Analysis for voltage divider bias

* Apply KVL to the collector-Emitter circuit

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

* Assume $I_E \simeq I_C$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$I_C = -\frac{1}{R_C + R_E} V_{CE} + \frac{V_{CC}}{R_C + R_E}$$

* This equation represents the dc load line with slope of $-\frac{1}{R_C + R_E}$ & y-intercept of $\frac{V_{CC}}{R_C + R_E}$

* When $I_C = 0$ ie the transistor is in cut-off region

$$V_{CE} = V_{CC}$$

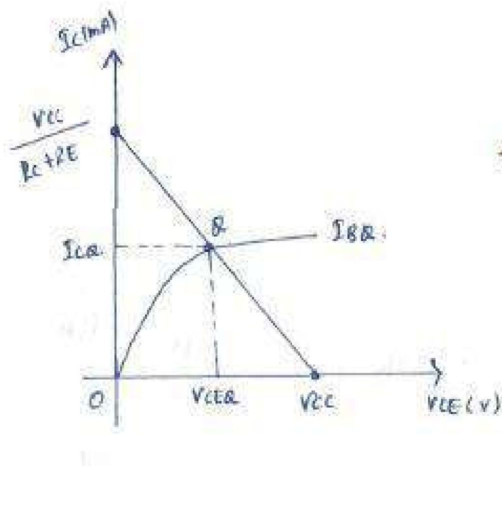
* When $V_{CE} = 0$ ie the transistor is in saturation region

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

* Thus the 2 end points are $(V_{CC}, 0)$ & $\left(0, \frac{V_{CC}}{R_C + R_E}\right)$ By joining these 2 end points, a DC load line is drawn

* From the base-emitter circuit

$$I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta) R_E}$$



* The saturation current for the circuit is $I_{C\,sat} = \frac{V_{CC}}{R_C + R_E}$

Bias compensation / Methods of stabilizing the Q-point

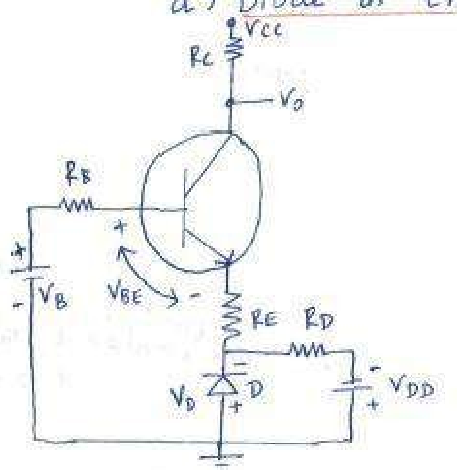
* The compensation Techniques uses Temperature sensitive devices such as diodes, Transistors. Thermistors etc.. to maintain the operating point constant.

1. Diode compensation Techniques
    1. compensation for V_{BE}
        a) Diode in Emitter circuit
        b) Diode in Voltage Divider circuit
    2. compensation for I_{co}
2. Thermistor Compensation Technique
3. Sensistor compensation Technique

1. Diode compensation Technique

1. compensation for V_{BE}

a) Diode in Emitter circuit



* Here, separate supply VDD is used to keep diode in Forward bias condition.

* If the diode & Transistor are of same material, the voltage across the Diode will have the same temperature coefficient ($-2.5\ mV/^\circ c$) as the V_{BE}.

* So the V_{BE} changes by ∂V_{BE} with change in temperature, V_D changes by ∂V_D & $\partial V_D' \simeq \partial V_{BE}$, the change tend to cancel each other.

* We know,

$$V_{BE} = V_T - \left[\frac{R_B + (1+\beta)R_E}{\beta}\right] I_c + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{co}$$

$$\left[\frac{R_B + (1+\beta)R_E}{\beta}\right] I_c = V_T - V_{BE} + \left[\frac{(R_E+R_B)(1+\beta)}{\beta}\right] I_{co}$$

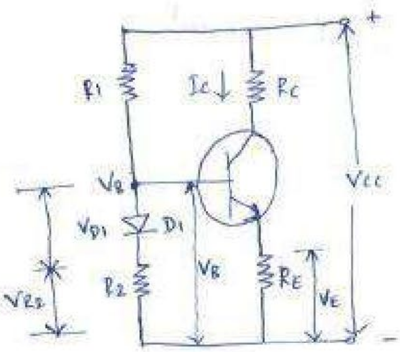
$$I_c = \frac{\beta[V_T - V_{BE}] + \cancel{\beta}\left[\frac{(R_E+R_B)(1+\beta)I_{co}}{\cancel{\beta}}\right]}{R_B + (1+\beta)R_E}$$

* We modify the equation

$$I_C = \frac{\beta\,[\,V - (V_{BE} - V_D)\,] + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

* I_C will be insensitive to variations in V_{BE}.

b) Diode in voltage Divider circuit



* Here, the diode is connected in series with resistance R_2 in the voltage divider circuit & it is in forward bias condition.
* We derived for voltage divider bias

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

also $I_E = \frac{V_E}{R_E}$ & $I_C \simeq I_E$.

$$I_C \simeq \frac{V_B - V_{BE}}{R_E} \quad \text{--- ①}$$

* When V_{BE} changes with temperature I_C also changes.
* The voltage at the base V_B is now

$$V_B = V_{R2} + V_D \quad \text{--- ②}$$

* sub eqn ② in ①

$$① \Rightarrow I_C \simeq \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

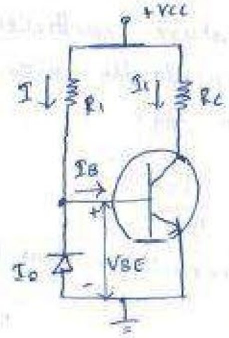
* If the diode & the Transistor are of the same type & material, the voltage across the diode will have the same temperature coefficient ($-2.5\,mV/°C$) as the VBE.
* So the VBE changes by ∂V_{BE} with change in temperature, V_D changes by ∂V_D & $\partial V_D \simeq \partial V_{BE}$. The change tend to cancel each other.
* The collector current as

$$I_C \simeq \frac{V_{R2}}{R_E}$$

* Which is unaffected due to change in VBE.
* The biasing is provided by R_1, R_2 & R_E.
* The change in V_{BE} due to temperature are compensated by changes in the diode voltage which keeps I_C stable at Q-point.

2. Compensation for I_{co} / Diode compensation for germanium Transistor

* In case of Ge, changes in I_{co} with Temperature are comparatively larger than Si Transistor.



* It plays more role in I_c stability than the change in VBE.
* It offers stabilization against variation in I_{co}.
* Here, the diode is kept in reverse bias condition
* In reverse bias condition the current flowing through diode is only the leakage current (I_o).

* If the diode & the Transistor are of the same type & material, the leakage current I_o of the diode will increase with temperature at the same rate as the collector leakage current I_{co}.

$$I = \frac{V_{cc} - V_{BE}}{R_1} \quad \& \quad I = I_B + I_o$$

$$\therefore \; I_B = I - I_o \quad \text{—} \; (1)$$

* For Ge Transistor $V_{BE} = 0.2\,V$, which is very small & neglecting change in V_{BE} with temperature.

* We can write

$$I \simeq \frac{V_{cc}}{R_1} \simeq \text{constant}$$

* We know

$$I_c = \beta I_B + (1+\beta) I_{co} \quad \text{—} \; (2)$$

sub (1) in (2)

$$(2) \Rightarrow \; I_c = \beta(I - I_o) + (1+\beta) I_{co}$$

$$= \beta I - \beta I_o + (1+\beta) I_{co}$$

* if $\beta >> 1$ we get

$$I_c = \beta I - \beta I_o + \beta I_{co}$$

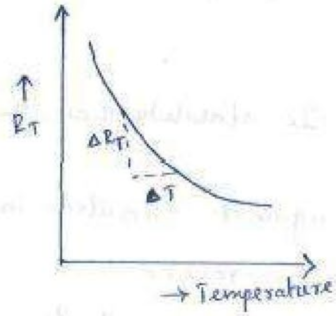
* We assume

$I_o = I_{co}$ we get

$$I_c = \beta I$$

* As I is constant, I_c remains fairly constant.
* We can say that changes by I_{co} with temperature are compensated by diode & thus collector current remains fairly constant.

2. Thermistor Compensation Technique

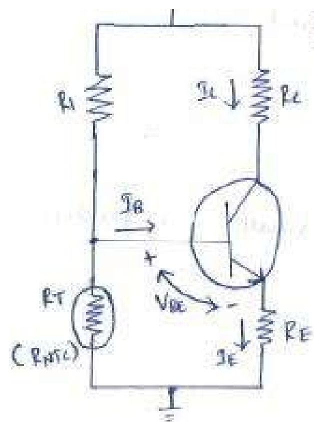


* This method uses Temperature sensitive devices such as Thermistors rather than diode (or) Transistor

* It has negative temperature coefficient. its resistance decreases exponentially with increasing Temperature: as shown in fig:

* Slope of this curve $= \frac{\partial R_T}{\partial T}$

* The $\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor has negative temperature coefficient resistance (NTC).



In This figure:

* R_2 is replaced by Thermistor R_T in self bias circuit.

* With increase in Temperature R_T decreases.

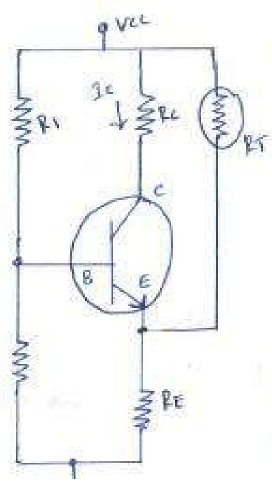
* Hence the voltage drop across it also decreases.

* The voltage drop is nothing but voltage at the base with respect to ground. Hence V_{BE} decreases which decrease I_B.

* This behaviour will tend to offset the increase in I_C with Temperature

* We know,

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$ → In this equation, There is increase in I_{CBO} & decrease in I_B which keeps I_C almost constant.



In This Fig:

* The Thermistor is connected b/w Emitter & V_{CC} to minimize the increase in I_C due to changes in I_{CO}, β (or) V_{BE} with Temperature.

* I_C increases with Temperature & R_T decreases with increase in Temperature.

* ∴ The current flow Through R_E increases, which increase the Voltage drop across it.

* The Emitter-Base junction is forward biased.

* But due to increase in Voltage drop across R_E, emitter is made more positive which decreases the forward bias Voltage V_{BE}.

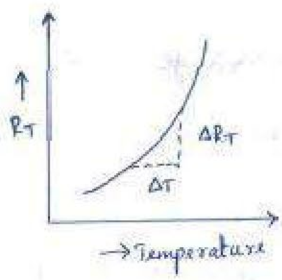
* Hence base current decreases.

* I_c is given by

$$I_c = \beta I_B + (1+\beta) I_{CBO}$$

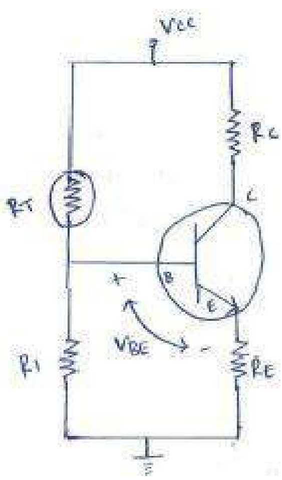
* As I_{CBO} increases with Temperature, I_B decreases & hence I_c remains fairly constant.

3. Sensistor compensation Technique



* This method uses temperature sensitive devices such as sensistor rather than diode (or) Transistor.
* It has a positive temperature coefficient. its resistance increases exponentially with increase temperature.

* slope of this curve $= \frac{\partial R_T}{\partial T}$
* $\frac{\partial R_T}{\partial T}$ is the temperature coefficient for sensistor & the slope is positive
* So we can say that sensistor have positive temperature coefficient of resistance (PTC)



In this Fig:

* R_1 is replaced by sensistor R_T in self bias circuit.
* Now R_T & R_2 are 2 resistors of the potential divider
* As temperature increases, R_T increases which decrease the current flowing through it.
* Hence the current through R_2 decreases which decrease the Voltage drop across it.
* Voltage drop across R_2 is the voltage b/w base & ground.
* So V_{BE} decreases which decreases I_B.

* $I_c = \beta I_B + (1+\beta) I_{CBO}$ → When I_{CBO} increases with increase in Temperature, I_B decreases due to reduction in V_{BE}, maintaining I_c fairly constant.

Thermal Stability

* The maximum average power $P_{D(max)}$ which a transistor can dissipate depends upon the transistor construction & may lie in the range from a few milliwatts to 200 W.

* The power dissipated ~~within~~ the transistor is predominantly the power dissipated at it's collector base junction.

* For Si transistor this temperature is in the range 150 to 225°C & for Ge transistor it's between 60 to 100°C.

* The collector - base junction temperature may rise because of 2 reasons.
  1. Due to rise in ambient temperature
  2. Due to self heating.

⇓

* The increase in collector current (I_C) increase the power dissipated at the collector junction. This in turn further increa the temperature of the junction & hence increase in the collector current (I_C). The process is cumulative & it's referred to as **Self heating.** The excess heat produced at the collector base junction may even burn & destroy the transistor. This situatic is called thermal runaway of the transistor.

2Mark

1. Thermal Resistance

* The stead state temperature rise at the collector junction is proportional to the power dissipated at the junction.

* It's given as

$$\partial T = T_j - T_A = \theta P_D \quad \text{—} ①$$

Where

T_j - Junction temperature in °C

T_A - Ambient temperature in °C.

P_D - Power in watts dissipated at the collector junction

θ - constant of proportionality.

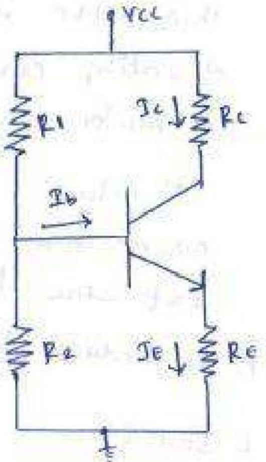
$$\frac{\partial P_D}{\partial T_j} = \frac{1}{\theta} \quad \text{--- (4)}$$

* substitute eqn 4 in (3) we get

$$\frac{\partial P_c}{\partial T_j} < \frac{1}{\theta} \quad \text{(5)}$$ → This condition must be satisfied to prevent Thermal runaway.

* By proper design of biasing circuit it's possible to ensure That the transistor can't runaway below a specified ambient temperature (or) even under any condition.

Voltage Divider Bias Circuit



* P_c = Heat generated at the collector junction.

= D.C power input to the circuit − power lost as I^2R in R_C & R_E

So

$$P_c = V_{CC} \times I_C - I_C^2 R_C - I_E^2 R_E \quad \text{--- (6)}$$

$\because I_C \cong I_E$

$$P_c = V_{CC} \times I_C - I_C^2 R_C - I_C^2 R_E$$

$$= V_{CC} \times I_C - I_C^2 (R_C + R_E) \quad \text{--- (7)}$$

* Differentiate eqn (7) w.r.to I_C we get

$$\frac{\partial P_c}{\partial I_C} = V_{CC} - 2 I_C (R_C + R_E) \quad \text{--- (8)}$$

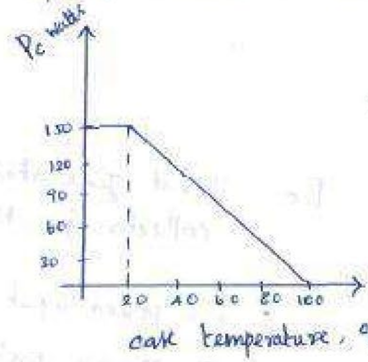
* Rewrite eqn (5)

$$\frac{\partial P_c}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta} \quad \text{--- (9)}$$

* The θ, which is constant of proportionality is referred to as Thermal resistance.

$$\theta = \frac{T_j - T_A}{P_D} \quad -(2)$$

* The unit of θ is Thermal resistance, is °c/watt.
* The θ various from 0.2°c/W for a high power transistor with an efficient heat sink to 1000°c/W for a low power transistor.
* The maximum collector power P_c allowed for safe operation is specified at 25°C.



→ * This curve is power - temperature derating curve for a germanium transistor.

* It shows that above 25°c, collector power must be decreased & at the extreme temperature at which the transistor may operate, P_c is reduced to zero.

2. Condition for Thermal Stability

* The Thermal runaway may even burn & destroy the transistor. it's necessary to avoid Thermal runaway.

2 Mark

* The required condition to avoid Thermal runaway is that the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated.

* It's given by

$$\frac{\partial P_c}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \quad -(3)$$

* Differentiate eqn (1) we get

$$T_j - T_A = \theta P_D \quad \text{w.r. to } T_j \text{ we get}$$

$$1 = \theta \frac{\partial P_D}{\partial T_j}$$

* The $\frac{\partial I_C}{\partial T_j}$ can be written as

$$\frac{\partial I_C}{\partial T_j} = S\frac{\partial I_{CO}}{\partial T_j} + S'\frac{\partial V_{BE}}{\partial T_j} + S''\frac{\partial \beta}{\partial T_j} \quad — (10)$$

* The junction temperature affect the I_C by affecting I_{CO}, V_{BE} & β.

* But for thermal runaway the affect of I_{CO} dominates.

$$\frac{\partial I_C}{\partial T_j} = \frac{\partial I_{CO}}{\partial T_j} \quad — (11)$$

* As the reverse saturation current (I_{CO}) for both Si & Ge transistor increases about 7% /°C.

$$\frac{\partial I_{CO}}{\partial T_j} = 0.07\, I_{CO} \quad — (12)$$

* substitute values of $\frac{\partial I_C}{\partial T_j}$ & $\frac{\partial P_C}{\partial I_C}$ in eqn (11) we get

$$\frac{\partial I_C}{\partial T_j} = S \times 0.07\, I_{CO} \quad — (13)$$

* Now substitute the values of $\frac{\partial I_C}{\partial T_j}$ & $\frac{\partial P_C}{\partial I_C}$ from eqn (13) & (8) in eqn (9) we get,

$$[V_{CC} - 2I_C(R_C+R_E)]\, S\,(0.07\, I_{CO}) < \frac{1}{\theta} \quad — (14)$$

$$\because V_{CC} < 2I_C(R_C+R_E)$$

$$\because \frac{V_{CC}}{2} < I_C(R_E+R_E) \quad — (15)$$

* Apply KVL to the collector-Emitter junction of voltage divider bias circuit we get

$$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0 \qquad \because I_C \simeq I_E$$

$$V_{CE} = V_{CC} - I_C(R_C+R_E)$$

$$I_C(R_C+R_E) = V_{CC} - V_{CE}$$

* Substitute value of $I_C(R_C+R_E)$ in eqn (15) we get

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

$$V_{CE} < \frac{V_{CC}}{2}$$

* Thus if $V_{CE} < \frac{V_{CC}}{2}$, The stability is ensured.

* But in transformer coupled circuit R_C & R_E are quite small & $V_{CE} \cong V_{CC}$.

* Hence it's necessary to design transformer coupled circuits with stability factor as close to 1 as possible to avoid thermal runaway.

Design of biasing for JFET

* FET - Field Effect Transistor - It's a semiconductor device which depends for its operation on the control of current by an electric field.

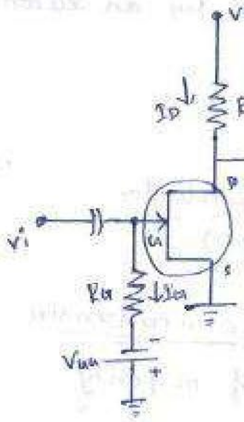
FET

- Junction field Effect Transistor (or) FET
- Metal-oxide-semiconductor Transistor (MOSFET)

FET differs from the BJT in the following characteristics

1. It's operation depends upon the flow of majority carriers only.
2. It's simpler to fabricate & occupies less space.
3. It exhibits a high input resistance, typically many mega ohms.
4. It's less noisy compared to BJT.
5. It exhibits no offset voltage at zero drain current

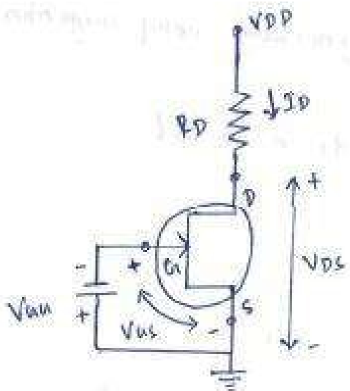
1. Fixed Bias | Gate Bias



* To make the gate-source junction reverse biased a separate supply V_{GG} is connected such that gate is more negative than the source.

Dc Analysis :

* For dc analysis coupling capacitors are open circuited.
* The current through R_G is I_G which is 0.
* This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit.



* We know for dc analysis

$$I_G = 0 \text{ amps}$$

* Apply KVL to the Gate to source junction

$$V_{GS} + V_{GG} = 0$$

$$\therefore V_{GS} = -V_{GG}$$

* Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude & hence the name fixed bias circuit

* For fixed bias circuit the I_D can be calculated as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

* Apply KVL to the Drain to Source junction

$$V_{DS} + I_D R_D - V_{DD} = 0$$

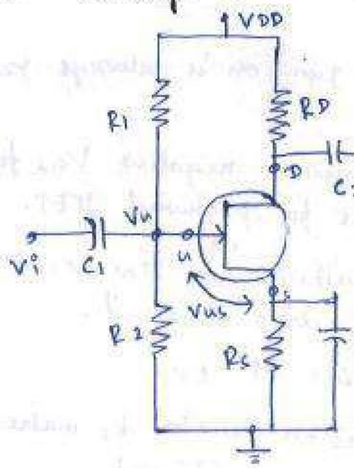
$$\therefore V_{DS} = V_{DD} - I_D R_D$$

Q-Point

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ} R_D$$

2. Voltage Divider Bias / potential Divider Bias



* The voltage at the source of the JFET must be more positive than the voltage at the Gate inorder to keep the Gate - source junction reverse biased.

* The source voltage is

$$V_S = I_S R_S \qquad \because I_S = I_D$$

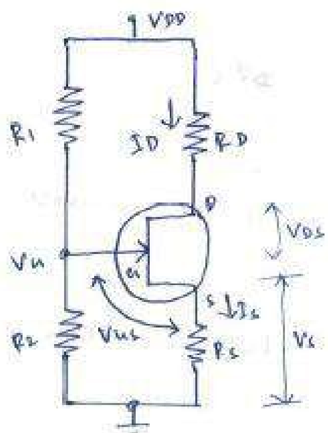
$$V_S = I_D R_S$$

* The Gate voltage is set by resistors R_1 & R_2 as expressed by the following equation using the voltage divider formula

$$V_G = \left(\frac{R_2}{R_1+R_2}\right) V_{DD} \qquad \because I_G = 0$$

Dc Analysis :

* For dc analysis the coupling capacitors are open circuited



* Apply KVL to the Gate - source junction

$$V_G - V_{GS} - V_S = 0$$

$$V_{GS} = V_G - V_S$$

$$= V_G - I_S R_S \qquad \because I_S = I_D$$

$$= V_G - I_D R_S$$

$$\therefore V_{GS} = V_G - I_D R_S$$

* Apply KVL to the Drain - Source Junction.

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - \overbrace{I_D R_S}^{V_S}$$

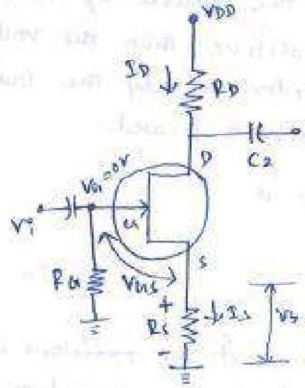
$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Q-point :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$$

3. Self Bias



* The Gate-source junction is always reverse biased.

* The condition requires negative V_{GS} for n-channel JFET & a positive V_{GS} for p-channel JFET.

* The R_G does not affect the bias because it has essentially no voltage drop across it.

* ∴ The Gate remains at 0V.

* The voltage drop across resistor R_s make the Gate-Source junction reverse biased.

* I_s produces voltage drop across R_s & make the source positive w.r.to ground.

Since

$$I_S = I_D \;\&\; V_G = 0 \quad \text{Then} \quad V_S = I_S R_S = I_D R_S$$

* The Gate-Source Voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

For p channel:

* The voltage drop across Rs & make the source negative w.r.t ground.

Since

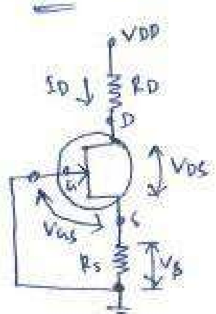
$$I_S = I_D \;\&\; V_G = 0 \quad \text{then} \quad V_S = -I_S R_S = -I_D R_S$$

* The Gate-Source Voltage is

$$V_{GS} = V_G - V_S = 0 - (-I_D R_S) = I_D R_S$$

DC Analysis:

For n-channel



For dc analysis the coupling capacitors are replaced by open circuit & R_G is replaced by short circuit equivalent, since $I_G = 0$.

W.K.T

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{—}①$$

Substitute the value of V_{GS} in eqn ①

$$① \Rightarrow I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2 \rightarrow \text{for n-channel}$$

$$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

Apply KVL to the Drain to source junction

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

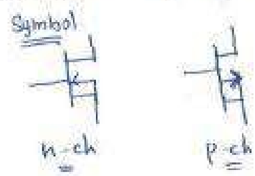
$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D$$

$$= V_{DD} - I_D R_S - I_D R_D$$

$$\therefore V_{DS} = V_{DD} - I_D(R_S + R_D)$$

Design of Biasing for MOSFET

* MOSFET - Metal Oxide Semiconductor Field Effect Transistor
* It has a Gate, Source & Drain like the JFET.
* The Drain current (I_D) in the MOSFET is controlled by the Gate-Source Voltage V_{GS}.



* There are 2 types of MOSFETS

  → Enhancement type (E-MOSFET)

  → Depletion type (D-MOSFET)

* MOSFET is also referred to as an IGATE because the gate is isolated from the channel.

1. DMOSFET

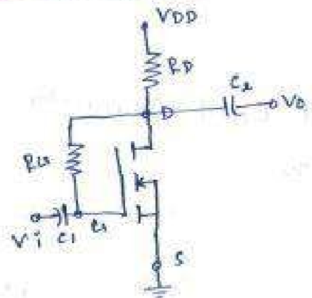
* It is similar to the circuit used for JFET biasing
* The primary difference b/w the two is the fact that depletion type MOSFETs also permits operating points with positive value of V_{GS} for n-channel & negative values of V_{GS} for p-channel.
* To have positive values of V_{GS} for n-channel & negative value of V_{GS} for p-channel self bias circuit is unsuitable.

[V_{GS} only
1. Fixed bias
2. Voltage divider bias]

2. EMOSFET

* It's similar to the circuit used for JFET biasing.
* The primary difference b/w the two is the fact that Enhancement type MOSFETS also permits operating points with positive value of V_{GS} for n-channel & negative values of V_{GS} for p-channel.
* To have positive values of V_{GS} the n-channel & negative value of V_{GS} for p-channel Self bias circuit is Unsuitable.
* Here, we will discuss only feedback bias & voltage divider bias circuit.

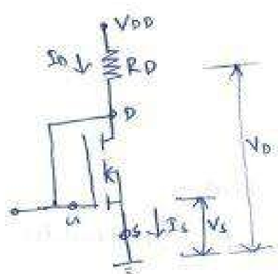
1. Feed Back Bias



Dc Analysis :

* For dc Analysis we can replace coupling capacitors by open circuit equivalent. Since $I_G = 0$. & replace the R_G by a short circuit equivalent.
* The Drain & Gate Terminals are shorted.

$$V_D = V_D \quad \& \quad V_{DS} = V_{GS} \quad \because V_S = 0$$



* Apply KVL to the Drain - source junction

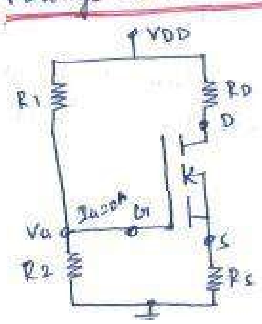
$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D$$

(or)

$$V_{GS} = V_{DD} - I_D R_D$$

2. Voltage Divider Bias



* The biasing resistors R_1 & R_2 are designed to provide positive gate to source voltage.
* Apply KVL to the Gate - Source junction

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S$$

$$V_{GS} = V_G - I_S R_S = V_G - I_D R_S \qquad \because I_D = I_S$$

$$\therefore V_{GS} = V_G - I_D R_S$$

* Apply KVL to Drain - source junction

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_S R_S$$

$$= V_{DD} - I_D R_D - I_D R_S \qquad \because I_D = I_S$$

$$\therefore V_{DS} = V_{DD} - I_D (R_D + R_S)$$

UNIT- V

BJT and FET Amplifiers

BJT: Two port network, Transistor hybrid model, determination of h-parameters, conversion of h-parameters, generalized analysis of transistor amplifier model using h-parameters, Analysis of CB, CE and CC amplifiers using exact and approximate analysis, Comparison of transistor amplifiers.**FET:** Generalized analysis of small signal model, Analysis of CG, CS and CD amplifiers, comparison of FET amplifiers.

Introduction:

In order to predict the behaviour of a small-signal transistor amplifier, it is important to know its operating characteristics *e.g.*, input impedance, output impedance, voltage gain *etc*. In the text so far, these characteristics were determined by using *β and circuit resistance values. This method of analysis has two principal advantages. Firstly, the values of circuit components are readily available and secondly the procedure followed is easily understood. However, the major drawback of this method is that accurate results cannot be obtained. It is because the input and output circuits of a transistor amplifier are not completely independent. For example, output current is affected by the value of load resistance rather than being constant at the value βI_b. Similarly, output voltage has an effect on the input circuit so that changes in the output cause changes in the input.

* Since transistor is generally connected in *CE* arrangement, current amplification factor β is mentioned here.

One of the methods that takes into account all the effects in a transistor amplifier is the hybrid parameter approach. In this method, four parameters (one measured in ohm, one in mho, two dimensionless) of a transistor are measured experimentally. These are called hybrid or *h* parameters of the transistor. Once these parameters for a transistor are known, formulas can be developed for input impedance, voltage gain etc.in terms of *h* parameters. There are two main reasons for using *h* parameter method in describing the characteristics of a transistor. Firstly, it yields exact results because the inter-effects of input and output circuits are taken into account. Secondly, these parameters can be measured very easily. To begin with, we shall apply *h* parameter approach to general circuits and then extend it to transistor amplifiers.

Hybrid Parameters:

*Every *linear circuit having input and output terminals can be analysed by four parameters (one measured in ohm, one in mho and two dimensionless) called* **hybrid** *or* ***h* Parameters.**

Hybrid means "mixed". Since these parameters have mixed dimensions, they are called hybrid parameters. Consider a linear circuit shown in Fig. 24.1. This circuit has input voltage and current labelled v_1 and i_1. This circuit also has output voltage and current labelled v_2 and i_2. Note that both input and output currents (i_1 and i_2) are assumed to flow *into* the box ; input and output voltages (v_1 and v_2) are assumed *positive* from the upper to the lower terminals. These are standard conventions and do not necessarily correspond to the actual directions and polarities. When we analyse circuits in which the voltages are of opposite polarity or where the currents flow out of the box, we simply treat these voltages and currents as negative quantities.

It can be proved by advanced circuit theory that voltages and currents in Fig. 24.1 can be related by the following sets of equations :

$$v_1 = h_{11} i_1 + h_{12} v_2 \quad ...(i)$$

$$i_2 = h_{21} i_1 + h_{22} v_2 \quad ...(ii)$$

In these equations, the hs are fixed constants for a given circuit and are called h parameters. Once these parameters are known, we can use equations (*i*) and (*ii*) to find the voltages and currents in the circuit. If we look at *eq.*(*i*), it is clear that **h_{11} has the dimension of ohm and h_{12} is dimensionless. Similarly, from *eq.* (*ii*), h_{21} is dimensionless and h_{22} has the dimension of mho. The following points may be noted about h parameters :

(*i*) Every linear circuit has four h parameters ; one having dimension of ohm, one having dimension of mho and two dimensionless.

(*ii*) The h parameters of a given circuit are constant. If we change the circuit, h parameters would also change.

(*iii*) Suppose that in a particular linear circuit, voltages and currents are related as under:

$$v_1 = 10i_1 + 6v_2$$
$$i_2 = 4i_1 + 3v_2$$

* A linear circuit is one in which resistances, inductances and capacitances remain fixed when voltage across them changes.

** The two parts on the R.H.S. of *eq.* (*i*) must have the unit of voltage. Since current (amperes) must be multiplied by resistance (ohms) to get voltage (volts), h_{11} should have the dimension of resistance *i.e.* ohms.

Here we can say that the circuit has h parameters given by $h_{11} = 10\,\Omega$; $h_{12} = 6$; $h_{21} = 4$ and $h_{22} = 3$ ℧.

Determination of h-parameters:

The major reason for the use of h parameters is the relative ease with which they can be measured. The h parameters of a circuit shown in Fig. 24.1 can be found out as under :

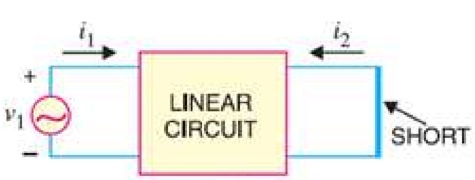
(*i*) If we short-circuit the output terminals (See Fig. 24.2), we can say that output voltage $v_2 = 0$. Putting $v_2 = 0$ in equations (*i*) and (*ii*), we get,

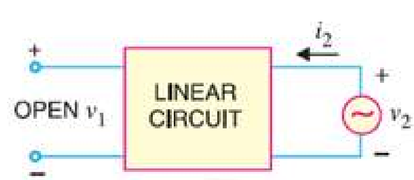
$$v_1 = h_{11}\, i_1 + h_{12} \times 0$$
$$i_2 = h_{21}\, i_1 + h_{22} \times 0$$

$$\therefore \quad h_{11} = \frac{v_1}{i_1} \quad \text{for } v_2 = 0 \text{ i.e. output shorted}$$

$$\text{and} \quad h_{21} = \frac{i_2}{i_1} \quad \text{for } v_2 = 0 \text{ i.e. output shorted}$$

Let us now turn to the physical meaning of h_{11} and h_{21}. Since h_{11} is a ratio of voltage and current (*i.e.* v_1/i_1), it is an impedance and is called * *"input impedance with output shorted"*. Similarly, h_{21} is the ratio of output and input current (*i.e.*, i_2/i_1), it will be dimensionless and is called *"current gain with output shorted"*.





(*ii*) The other two h parameters (*viz* h_{12} and h_{22}) can be found by making $i_1 = 0$. This can be done by the arrangement shown in Fig. Here, we drive the output terminals with voltage v_2, keeping the input terminals open. With this set up, $i_1 = 0$ and the equations become :

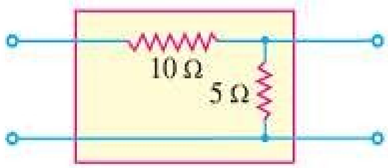
$$v_1 = h_{11} \times 0 + h_{12}\, v_2$$
$$i_2 = h_{21} \times 0 + h_{22}\, v_2$$

$\therefore \qquad h_{12} = \dfrac{v_1}{v_2} \quad$ for $i_1 = 0$ *i.e.* input open

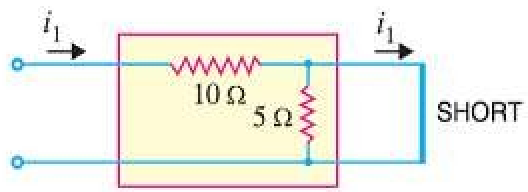
and $\qquad h_{22} = \dfrac{i_2}{v_2} \quad$ for $i_1 = 0$ *i.e.* input open

Since h_{12} is a ratio of input and output voltages (*i.e.* v_1/v_2), it is dimensionless and is called *"voltage feedback ratio with input terminals open"*. Similarly, h_{22} is a ratio of output current and output voltage (*i.e.* i_2/v_2), it will be admittance and is called *"output admittance with input terminals open"*.

Example. *Find the h parameters of the circuit shown in Fig.*



(*i*)



(*ii*)

* Note that v_1 is the input voltage and i_1 is the input current. Hence v_1/i_1 is given the name input impedance.

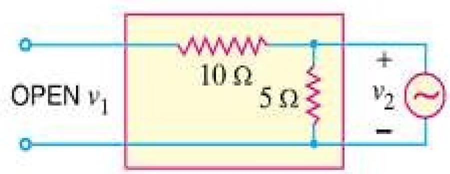
Solution. The h parameters of the circuit shown in Fig. can be found as under :

To find h_{11} and h_{21}, short - circuit the output terminals as shown in Fig. It is clear that input impedance of the circuit is 10 Ω because 5 Ω resistance is shorted out.

$\therefore \qquad h_{11} = \mathbf{10\ \Omega}$

Now current i_1 flowing into the box will flow through 10 Ω resistor and then through the shorted path as shown. It may be noted that in our discussion, i_2 is the output current flowing into the box. Since output current in Fig. is actually flowing out of the box, i_2 is negative *i.e.*,

$$i_2 = -i_1$$
$$h_{21} = \frac{i_2}{i_1} = \frac{-i_1}{i_1} = \mathbf{-1}$$



(*iii*)

To find h_{12} and h_{22}, make the arrangement as shown in Fig. (*iii*). Here we are driving the output terminals with a voltage v_2. This sets up a current i_2. Note that input terminals are open. Under this condition, there will be no current in 10Ω resistor and, therefore, there can be no voltage drop across it. Consequently, all the voltage appears across input terminals *i.e.*

$$v_1 = v_2$$

$$\therefore \quad h_{12} = \frac{v_1}{v_2} = \frac{v_2}{v_2} = \mathbf{1}$$

Now the output impedance looking into the output terminals with input terminals open is simply 5 Ω. Then h_{22} will be the reciprocal of it because h_{22} is the output admittance with input terminals open.

$$\therefore \quad h_{22} = 1/5 = \mathbf{0.2 ℧}$$

The h parameters of the circuit are :

$$h_{11} = 10\,\Omega \;;\; h_{21} = -1$$

$$h_{12} = 1 \;;\; h_{22} = 0.2\,℧$$

It may be mentioned here that in practice, dimensions are not written with h parameters. It is because it is understood that h_{11} is always in ohms, h_{12} and h_{21} are dimensionless and h_{22} is in mhos.

Example *Find the h parameters of the circuit shown in Fig.*

(*i*) (*ii*)

Solution. First of all imagine that output terminals are short-circuited as shown in Fig. (*ii*). The input impedance under this condition is the parameter h_{11}.

Obviously, $$h_{11} = 4 + 4 \parallel 4$$

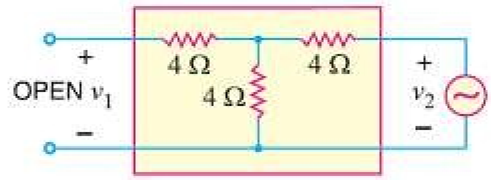
$$= 4 + \frac{4 \times 4}{4 + 4} = \mathbf{6\,\Omega}$$

Now the input current i_1 in Fig. (*ii*) will divide equally at the junction of 4 Ω resistors so that output current is $i_1/2$ *i.e.*

$$i_2 = -i_1/2 = -0.5\, i_1$$

$$\therefore \qquad h_{21} = \frac{i_2}{i_1} = \frac{-0.5\, i_1}{i_1} = -\mathbf{0.5}$$

In order to find h_{12} and h_{22}, imagine the arrangement as shown in Fig. (*iii*). Here we are driving the output terminals with voltage v_2, keeping the input terminals open. Under this condition, any voltage v_2 applied to the output will divide by a factor 2 *i.e.*



(*iii*)

$$v_1 = \frac{v_2}{2} = 0.5\, v_2$$

$$\therefore \qquad h_{12} = \frac{v_1}{v_2} = \frac{0.5\, v_2}{v_2} = \mathbf{0.5}$$

Now the output impedance looking into the output terminals with input terminals open is simply 8 Ω. Then h_{22} will be the reciprocal of this *i.e.*

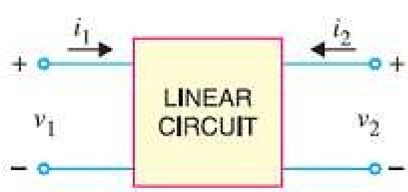
$$h_{22} = \frac{1}{8} = \mathbf{0.125\ \mho}$$

h-parameter equivalent circuit:

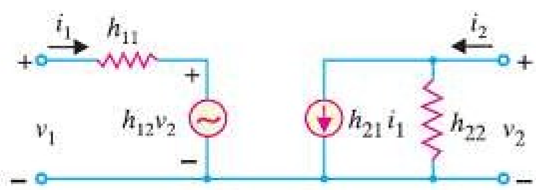
Fig. (*i*) shows a linear circuit. It is required to draw the h parameter equivalent circuit of Fig. (*i*). We know that voltages and currents of the circuit in Fig. (*i*) can be expressed in terms of h parameters as under :

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2 \qquad ...(i)$$

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2 \qquad ...(ii)$$



(*i*)



(*ii*)

Fig. (*ii*) shows h parameter equivalent circuit of Fig. (*i*) and is derived from equations (*i*) and (*ii*). The *input circuit* appears as a resistance h_{11} in series with a voltage generator $h_{12}\, v_2$. This circuit is derived from equation (*i*). The *output circuit* involves two components ; a current generator $h_{21}\, i_1$ and shunt resistance h_{22} and is derived from equation (*ii*). The following points are worth noting about the h parameter equivalent circuit

(*i*) This circuit is called hybrid equivalent because its input portion is a Thevenin equivalent, or voltage generator with series resistance, while output side is Norton equivalent, or current generator with shunt resistance. Thus it is a mixture or a hybrid. The symbol 'h' is simply the abbreviation of the word hybrid (hybrid means "mixed").

(*ii*) The different hybrid parameters are distinguished by different number subscripts. The notation shown in Fig. (*ii*) is used in general circuit analysis. The first number designates the circuit in which the effect takes place and the second number designates the circuit from which the effect comes. For instance, h_{21} is the "short-circuit forward current gain" or the ratio of the current in the output (*circuit* 2) to the current in the input (*circuit* 1).

(*iii*) The equivalent circuit of Fig. (*ii*) is extremely useful for two main reasons. First, it isolates the input and output circuits, their interaction being accounted for by the two controlled sources. Thus, the effect of output upon input is represented by the equivalent voltage generator $h_{12}v_2$ and its value depends upon output voltage. Similarly, the effect of input upon output is represented by current generator $h_{21}i_1$ and its value depends upon input current. Secondly, the two parts of the circuit are in a form which makes it simple to take into account source and load circuits.

Performance of a linear circuit in h-parameters:

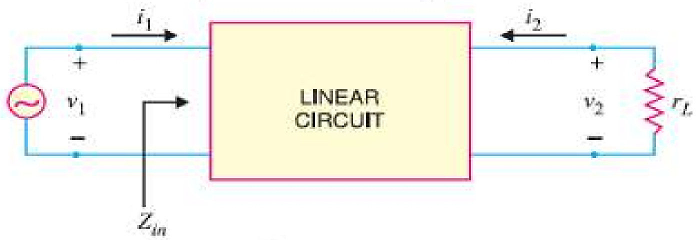
We have already seen that any linear circuit with input and output has a set of h parameters. We shall now develop formulas for input impedance, current gain, voltage gain etc.of a linear circuit in terms of h parameters.

(*i*) **Input impedance.** Consider a linear circuit with a load resistance r_L across its terminals as shown in Fig. . The input impedance Z_{in} of this circuit is the ratio of input voltage to input current *i.e.*

$$Z_{in} = \frac{v_1}{i_1}$$

Now $v_1 = h_{11}\, i_1 + h_{12}\, v_2$ in terms of h parameters. Substituting the value of v_1 in the above expression, we get,

$$Z_{in} = \frac{h_{11}\, i_1 + h_{12}\, v_2}{i_1} = h_{11} + \frac{h_{12}\, v_2}{i_1} \qquad ...(i)$$



Now, $i_2 = h_{21}\, i_1 + h_{22}\, v_2$ in terms of h parameters. Further from Fig. it is clear that $i_2 = -v_2/r_L$. The minus sign is used here because the actual load current is opposite to the direction of i_2.

$$\therefore \qquad \frac{-v_2}{r_L} = h_{21}\, i_1 + h_{22}\, v_2 \qquad \left[\because i_2 = \frac{-v_2}{r_L}\right]$$

$$\text{or} \qquad -h_{21}\, i_1 = h_{22}\, v_2 + \frac{v_2}{r_L} = v_2\left(h_{22} + \frac{1}{r_L}\right)$$

$$\therefore \qquad \frac{v_2}{i_1} = \frac{-h_{21}}{h_{22} + \frac{1}{r_L}} \qquad ...(ii)$$

Substituting the value of v_2/i_1 from exp. (*ii*) into exp. (*i*), we get,

$$\mathbf{Z_{in}} = h_{11} - \frac{h_{12}\, h_{21}}{h_{22} + \frac{1}{r_L}} \qquad ...(iii)$$

This is the expression for input impedance of a linear circuit in terms of h parameters and load connected to the output terminals. If either h_{12} or r_L is very small, the second term in exp. (*iii*) can be neglected and input impedance becomes :

$$\mathbf{Z_{in}} = h_{11}$$

(ii) **Current Gain.** Referring to Fig. , the current gain A_i of the circuit is given by :

$$A_i = \frac{i_2}{i_1}$$

Now $$i_2 = h_{21}\, i_1 + h_{22}\, v_2$$

and $$v_2 = -\,i_2\, r_L$$

$\therefore$ $$i_2 = h_{21}\, i_1 - h_{22}\, i_2\, r_L$$

or $$i_2\,(1 + h_{22}\, r_L) = h_{21}\, i_1$$

or $$\frac{i_2}{i_1} = \frac{h_{21}}{1 + h_{22}\; r_L}$$

But $i_2/i_1 = A_i$, the current gain of the circuit.

$\therefore$ $$\mathbf{A_i} = \frac{h_{21}}{1 + h_{22}\; r_L}$$

If $h_{22}\, r_L << 1$, then $A_i \simeq h_{21}$.

The expression $A_i \simeq h_{21}$ is often useful. To say that $h_{22}\, r_L << 1$ is the same as saying that $r_L << 1/h_{22}$. This occurs when r_L is much smaller than the output resistance $(1/h_{22})$, shunting $h_{21}\, i_1$ generator. Under such condition, most of the generator current bypasses the circuit output resistance in favour of r_L. This means that $i_2 \simeq h_{21}\, i_1$ or $i_2/i_1 \simeq h_{21}$.

(iii) **Voltage gain.** Referring back to Fig. , the voltage gain of the circuit is given by :

$$A_v = \frac{v_2}{v_1}$$

$$= \frac{v_2}{i_1\, Z_{in}} \qquad (\because\; v_1 = i_1 Z_{in}) \qquad ...(iv)$$

While developing expression for input impedance, we found that :

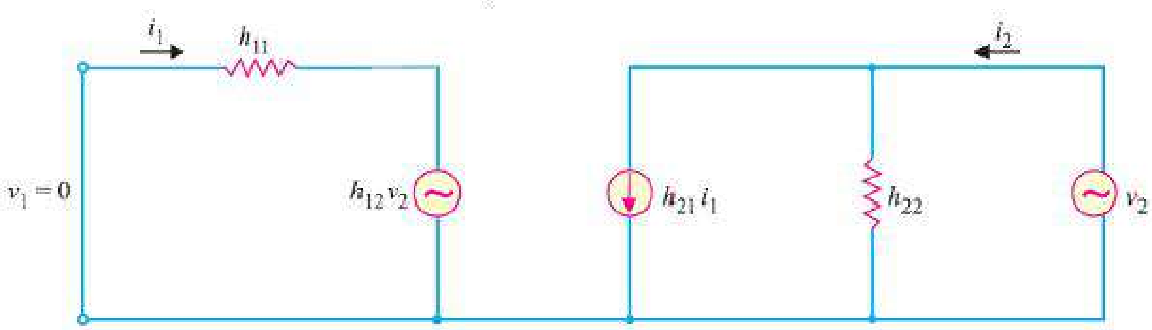
$$\frac{v_2}{i_1} = \frac{-\,h_{21}}{h_{22} + \frac{1}{r_L}}$$

Substituting the value of v_2/i_1 in exp. *(iv)*, we get,

$$\mathbf{A_v} = \frac{-\,h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_L}\right)}$$

(iv) **Output impedance.** In order to find the output impedance, remove the load r_L, set the signal voltage v_1 to zero and connect a generator of voltage v_2 at the output terminals. Then h parameter equivalent circuit becomes as shown in Fig. By definition, the output impedance Z_{out} is

$$Z_{out} = \frac{v_2}{i_2}$$



With $v_1 = 0$ and applying Kirchhoff's voltage law to the input circuit, we have,

$$0 = i_1 h_{11} + h_{12} v_2$$

$$\therefore \quad i_1 = -\frac{h_{12} v_2}{h_{11}}$$

Now $$i_2 = h_{21} i_1 + h_{22} v_2$$

Putting the value of i_1 $(= -h_{12} v_2/h_{11})$ in this equation, we get,

$$i_2 = h_{21}\left(-\frac{h_{12} v_2}{h_{11}}\right) + h_{22} v_2$$

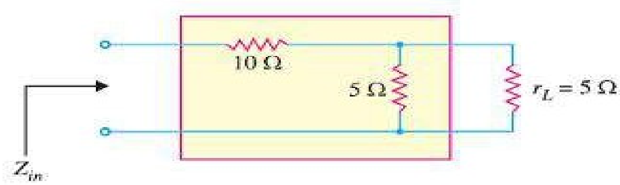
or $$i_2 = -\frac{h_{21} h_{12} v_2}{h_{11}} + h_{22} v_2$$

Dividing throughout by v_2, we have,

$$\frac{i_2}{v_2} = \frac{-h_{21} h_{12}}{h_{11}} + h_{22}$$

$$\therefore \quad Z_{out} = \frac{v_2}{i_2} = \frac{1}{h_{22} - \dfrac{h_{21} h_{12}}{h_{11}}}$$

Example *Find the (i) input impedance and (ii) voltage gain for the circuit shown in*



Solution. The h parameters of the circuit inside the box are the same as those calculated in example

$$h_{11} = 10; \quad h_{21} = -1$$
$$h_{12} = 1 \quad \text{and} \quad h_{22} = 0.2$$

(*i*) Input impedance is given by :

$$Z_{in} = h_{11} - \frac{h_{12} h_{21}}{h_{22} + \dfrac{1}{r_L}} = 10 - \frac{1 \times -1}{0.2 + \dfrac{1}{5}}$$

$$= 10 + 2.5 = \mathbf{12.5\ \Omega}$$

By inspection, we can see that input impedance is equal to 10 Ω plus two 5 Ω resistances in parallel *i.e.*

$$Z_{in} = 10 + 5 \,||\, 5$$

$$= 10 + \frac{5 \times 5}{5 + 5} = 12.5\ \Omega$$

(*ii*) Voltage gain, $$A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \dfrac{1}{r_L}\right)} = \frac{1}{12.5\left(0.2 + \dfrac{1}{5}\right)} = \mathbf{\frac{1}{5}}$$

It means that output voltage is one-fifth of the input voltage. This can be readily established by inspection of Fig. The two 5 Ω resistors in parallel give a net resistance of 2.5 Ω. Therefore, we have a voltage divider consisting of 10 Ω resistor in series with 2.5 Ω resistor.

$$\therefore \quad \text{Output voltage} = \frac{2.5}{12.5} \times \text{Input voltage}$$

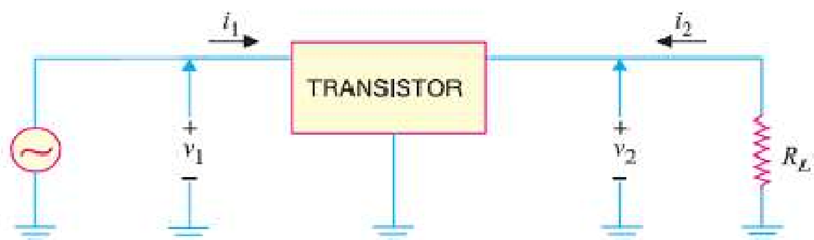
$$\text{or} \quad \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{2.5}{12.5} = \frac{1}{5}$$

$$\text{or} \quad A_v = \frac{1}{5}$$

Comments. The reader may note that in a simple circuit like that of Fig. , it is not advisable to use *h* parameters to find the input impedance and voltage gain. It is because answers of such circuits can be found directly by inspection. However, in complicated circuits, inspection method becomes cumbersome and the use of *h* parameters yields quick results.

h-parameters of a transistor:

It has been seen in the previous sections that every linear circuit is associated with *h* parameters. When this linear circuit is terminated by load r_L, we can find input impedance, current gain, voltage gain, etc. in terms of *h* parameters. Fortunately, for *small* a.c. signals, the transistor behaves as a linear device because the output a.c. signal is directly proportional to the input a.c. signal. Under such circumstances, the a.c. *operation* of the transistor can be described in terms of *h* parameters. The expressions derived for input impedance, voltage gain *etc.* in the previous section shall hold good for transistor amplifier except that here r_L is the a.c. load seen by the transistor.



shows the transistor amplifier circuit. There are four quantities required to describe the external behaviour of the transistor amplifier. These are v_1, i_1, v_2 and i_2 shown on the diagram of Figure These voltages and currents can be related by the following sets of equations :

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2$$
$$i_2 = h_{21}\, i_1 + h_{22}\, v_2$$

The following points are worth noting while considering the behaviour of transistor in terms of *h* parameters :

(*i*) For small a.c. signals, a transistor behaves as a linear circuit. Therefore, its a.c. operation can be described in terms of *h* parameters.

(*ii*) The value of *h* parameters of a transistor will depend upon the transistor connection (*i.e. CB, CE* or *CC*) used. For instance, a transistor used in *CB* arrangement may have $h_{11} = 20\ \Omega$. If we use the same transistor in *CE* arrangement, h_{11} will have a different value. Same is the case with other *h* parameters.

(*iii*) The expressions for input impedance, voltage gain etc. derived in Figure are also applicable to transistor amplifier except that r_L is the a.c. load seen by the transistor *i.e.*

$$r_L = R_C \,||\, R_L$$

(*iv*) The values of h parameters depend upon the operating point. If the operating point is changed, parameter values are also changed.

(*v*) The notations v_1, i_1, v_2 and i_2 are used for general circuit analysis. In a transistor amplifier, we use the notation depending upon the configuration in which transistor is used. Thus for *CE* arrangement,

$$v_1 = V_{be} \quad ; \quad i_1 = I_b \quad ; \quad v_2 = V_{ce} \quad ; \quad i_2 = I_c$$

Here V_{be}, I_b, V_{ce} and I_c are the R.M.S. values.

Nomenclature for Transistor h-parameters:

The numerical subscript notation for h parameters (*viz.* h_{11}, h_{21}, h_{12} and h_{22}) is used in general circuit analysis. However, this nomenclature has been modified for a transistor to indicate the nature of parameter and the transistor configuration used. The h parameters of a transistor are represented by the following notation :

(*i*) The numerical subscripts are replaced by letter subscripts.

(*ii*) The first letter in the double subscript notation indicates the nature of parameter.

(*iii*) The second letter in the double subscript notation indicates the circuit arrangement (*i.e.* *CB*, *CE* or *CC*) used.

Table below shows the h parameter nomenclature of a transistor :

S.No.	*h* parameter	Notation in CB	Notation in CE	Notation in CC
1.	h_{11}	h_{ib}	h_{ie}	h_{ic}
2.	h_{12}	h_{rb}	h_{re}	h_{rc}
3.	h_{21}	h_{fb}	h_{fe}	h_{fc}
4.	h_{22}	h_{ob}	h_{oe}	h_{oc}

Note that first letter *i*, *r*, *f* or *o* indicates the nature of parameter. Thus h_{11} indicates input impedance and this parameter is designated by the subscript *i*. Similarly, letters *r*, *f* and *o* respectively indicate reverse voltage feedback ratio, forward current transfer ratio and output admittance. The second letters *b*, *e* and *c* respectively indicate *CB*, *CE* and *CC* arrangement.

Transistor Circuit Performance in h-parameters:

The expressions for input impedance, voltage gain etc. in terms of h parameters derived in **Figure** for general circuit analysis apply equally for transistor analysis. However, it is profitable to rewrite them in standard transistor h parameter nomenclature.

(*i*) **Input impedance.** The general expression for input impedance is

$$Z_{in} = h_{11} - \frac{h_{12}\ h_{21}}{h_{22} + \frac{1}{r_L}}$$

Using standard h parameter nomenclature for transistor, its value for *CE* arrangement will be :

$$Z_{in} = h_{ie} - \frac{h_{re}\ h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

Similarly, expressions for input impedance in *CB* and *CC* arrangements can be written. It may be noted that r_L is the a.c. load seen by the transistor.

(*ii*) **Current gain.** The general expression for current gain is

$$A_i = \frac{h_{21}}{1 + h_{22}\ r_L}$$

Using standard transistor h parameter nomenclature, its value for CE arrangement is

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

The reader can readily write down the expressions for CB and CC arrangements.

(iii) Voltage gain. The general expression for voltage gain is

$$A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_L}\right)}$$

Using standard transistor h parameter nomenclature, its value for CE arrangement is

$$A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

In the same way, expressions for voltage gain in CB and CC arrangement can be written.

(iv) Output impedance. The general expression for output impedance is

$$Z_{out} = \frac{1}{h_{22} - \frac{h_{21}\, h_{12}}{h_{11}}}$$

Using standard transistors h parameter nomenclature, its value for CE arrangement is

$$Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}\, h_{re}}{h_{ie}}}$$

In the same way, expression for output impedance in CB and CC arrangements can be written.

The above expression for Z_{out} is for the transistor. If the transistor is connected in a circuit to form a single stage amplifier, then output impedance of the stage $= Z_{out} \parallel r_L$ where $r_L = R_C \parallel R_L$.

Example *A transistor used in CE arrangement has the following set of h parameters when the d.c. operating point is V_{CE} = 10 volts and I_C = 1 mA :*

$h_{ie} = 2000\ \Omega;\quad h_{oe} = 10^{-4}$ mho; $\quad h_{re} = 10^{-3};\quad h_{fe} = 50$

Determine (i) input impedance (ii) current gain and (iii) voltage gain. The a.c. load seen by the transistor is $r_L = 600\ \Omega$. What will be approximate values using reasonable approximations?

Solution. (*i*) Input impedance is given by :

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 2000 - \frac{10^{-3} \times 50}{10^{-4} + \frac{1}{600}} \quad \text{.... } (i)$$

$$= 2000 - 28 = \mathbf{1972\ \Omega}$$

The second term in eq. (*i*) is quite small as compared to the first.

$\therefore \quad Z_{in} \simeq h_{ie} = \mathbf{2000\ \Omega}$

(*ii*) Current gain, $A_i = \dfrac{h_{fe}}{1 + h_{oe} \times r_L} = \dfrac{50}{1 + (600 \times 10^{-4})} = \mathbf{47}$

If $h_{oe}\, r_L << 1$, then $A_i \simeq h_{fe} = \mathbf{50}$

(*iii*) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)} = \dfrac{-50}{1972\left(10^{-4} + \frac{1}{600}\right)} = \mathbf{-14.4}$

The negative sign indicates that there is 180° phase shift between input and output. The magnitude of gain is 14.4. In other words, the output signal is 14.4 times greater than the input and it is 180° out of phase with the input.

Example *A transistor used in CE connection has the following set of h parameters when the d.c. operating point is V_{CE} = 5 volts and I_C = 1 mA :*

h_{ie} = 1700 Ω; h_{re} = 1.3×10^{-4}; h_{fe} = 38; h_{oe} = 6×10^{-6} ℧

If the a.c. load r_L seen by the transistor is 2 kΩ, find (i) the input impedance (ii) current gain and (iii) voltage gain.

Solution. (*i*) The input impedance looking into the base of transistor is

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 1700 - \frac{1.3 \times 10^{-4} \times 38}{6 \times 10^{-6} + \frac{1}{2000}} \simeq \mathbf{1690\ \Omega}$$

(*ii*) Current gain, $A_i = \dfrac{h_{fe}}{1 + h_{oe} r_L} = \dfrac{38}{1 + 6 \times 10^{-6} \times 2000} = \dfrac{38}{1.012} \simeq \mathbf{37.6}$

(*iii*) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \dfrac{1}{r_L}\right)} = \dfrac{-38}{1690\left(6 \times 10^{-6} + \dfrac{1}{2000}\right)} = \mathbf{44.4}$

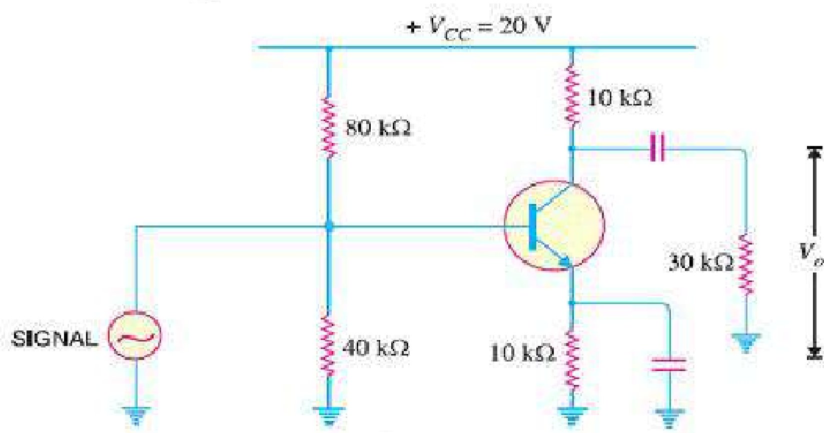
Example *Fig. shows the transistor amplifier in CE arrangement. The h parameters of transistor are as under :*

h_{ie} = 1500 Ω; h_{fe} = 50; h_{re} = 4×10^{-4}; h_{oe} = 5×10^{-5} ℧

Find (i) a.c. input impedance of the amplifier (ii) voltage gain and (iii) output impedance.

Solution. The a.c. load r_L seen by the transistor is equivalent of the parallel combination of R_C (= 10 kΩ) and R_L (= 30 kΩ) *i.e.*

$$r_L = \frac{R_C R_L}{R_C + R_L} = \frac{10 \times 30}{10 + 30} = 7.5\ \text{k}\Omega = 7500\ \Omega$$



(*i*) The input impedance looking into the base of transistor is given by :

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 1500 - \frac{4 \times 10^{-4} \times 50}{5 \times 10^{-5} + \frac{1}{7500}} = 1390\ \Omega$$

This is only the input impedance looking into the base of transistor. The a.c. input impedance of the entire stage will be Z_{in} in parallel with bias resistors *i.e.*

Input impedance of stage = $80 \times 10^3 \,||\, 40 \times 10^3 \,||\, 1390 =$ **1320 Ω**

(ii) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \dfrac{1}{r_L}\right)} = \dfrac{-50}{1390\left(5 \times 10^{-5} + \dfrac{1}{7500}\right)} = \mathbf{-196}$

The negative sign indicates phase reversal. The magnitude of gain is 196.

(iii) Output impedance of transistor is

$$Z_{out} = \frac{1}{h_{oe} - \dfrac{h_{fe}\, h_{re}}{h_{ie}}}$$

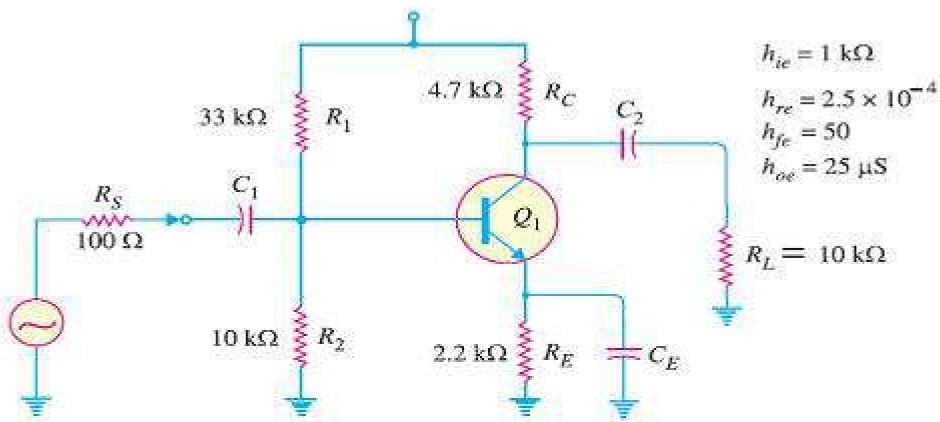
$$= \frac{1}{5 \times 10^{-5} - \dfrac{50 \times 4 \times 10^{-4}}{1500}} = 27270\,\Omega = 27.27\,\text{k}\Omega$$

∴ Output impedance of the stage

$$= Z_{out} \,||\, R_L \,||\, R_C$$

$$= 27.27\,\text{k}\Omega \,||\, 30\,\text{k}\Omega \,||\, 10\,\text{k}\Omega = \mathbf{5.88\,k\Omega}$$

Example *Find the value of current gain for the circuit shown in Fig . The h-parameter values of the transistor are given alongside the figure.*



Solution. The current gain A_i for the circuit is given by ;

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

Here $r_L = R_C \,||\, R_L = 4.7\,\text{k}\Omega \,||\, 10\,\text{k}\Omega = 3.2\,\text{k}\Omega$

∴ $A_i = \dfrac{50}{1 + (25 \times 10^{-6})(3.2 \times 10^3)} = \mathbf{46.3}$

Note that current gain of the circuit is very close to the value h_{fe}. The reason for this is that $h_{oe}\, r_L << 1$. Since this is normally the case, $A_i \simeq h_{fe}$.

Example *In the above example, determine the output impedance of the transistor.*

Solution. Note that the signal source (See Fi) has resistance $R_S = 100\,\Omega$.

∴ Output impedance Z_{out} of the transistor is

$$Z_{out} = \frac{1}{h_{oe} - \left(\dfrac{h_{fe}\, h_{re}}{h_{ie} + R_S}\right)}$$

$$= \frac{1}{(25 \times 10^{-6}) - \dfrac{(50)\,(2.5 \times 10^{-4})}{(1 \times 10^{3}) + 100}} = 73{\cdot}3 \times 10^{3}\ \Omega = \mathbf{73.3\ k\Omega}$$

Approximate hybrid model of Transistor amplifier:

The h-parameter formulas (CE configuration) covered in can be approximated to a form that is easier to handle. While these approximate formulas will not give results that are as accurate as the original formulas, they can be used for many applications.

(*i*) Input impedance

Input impedance, $Z_{in} = h_{ie} - \dfrac{h_{re}\, h_{fe}}{h_{oe} + \dfrac{1}{r_L}}$

In actual practice, the second term in this expression is very small as compared to the first term.

$\therefore \quad Z_{in} = h_{ie}$ ... approximate formula

(*ii*) Current gain

Current gain, $A_i = \dfrac{h_{fe}}{1 + h_{oe}\, r_L}$

In actual practice, $h_{oe}\, r_L$ is very small as compared to 1.

$\therefore \quad A_i = h_{fe}$ ... approximate formula

(*iii*) Voltage gain

$$\text{Voltage gain, } A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \dfrac{1}{r_L}\right)}$$

$$= \frac{-h_{fe}\, r_L}{Z_{in}\,(h_{oe}\, r_L + 1)}$$

Now approximate formula for Z_{in} is h_{ie}. Also $h_{oe}\, r_L$ is very small as compared to 1.

$\therefore \quad A_v = -\dfrac{h_{fe}\, r_L}{h_{ie}}$ ... approximate formula

(*iv*) Output impedance

Output impedance of transistor, $Z_{out} = \dfrac{1}{h_{oe} - \dfrac{h_{fe}\, h_{re}}{h_{ie}}}$

The second term in the denominator is very small as compared to h_{oe}.

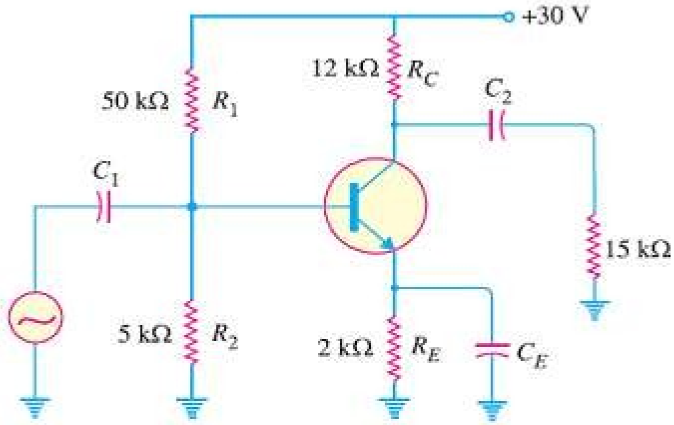
$\therefore \quad Z_{out} = \dfrac{1}{h_{oe}}$ ... approximate formula

The output impedance of transistor amplifier

$= Z_{out} \parallel r_L$ where *$r_L = R_C \parallel R_L$

If the amplifier is unloaded (*i.e.* $R_L = \infty$), $r_L = R_C$.

Example *For the circuit shown in Fig. use approximate hybrid formulas to determine (i) the input impedance (ii) voltage gain. The h parameters of the transistor are h_{ie} = 1.94 kΩ and h_{fe} = 71.*



Solution.

a.c. collector load, $r_L = R_C \| R_L = 12\ k\Omega \| 15\ k\Omega = 6.67\ k\Omega$

(*i*) Transistor input impedance is

$$Z_{in\ (base)} = h_{ie} = 1.94\ k\Omega$$

∴ Circuit input impedance $= Z_{in\ (base)} \| R_1 \| R_2$

$$= 1.94\ k\Omega \| 50\ k\Omega \| 5\ k\Omega = \mathbf{1.35\ k\Omega}$$

(*ii*) Voltage gain, $A_v = \dfrac{h_{fe}\, r_L}{h_{ie}} = \dfrac{71 \times 6.67\ k\Omega}{1.94\ k\Omega} = \mathbf{244}$

Example *A transistor used in an amplifier has h-parameter values of h_{ie} = 600 Ω to 800Ω and h_{fe} = 110 to 140. Using approximate hybrid formula, determine the voltage gain for the circuit. The a.c. collector load, r_L = 460 Ω.*

Solution. When *minimum* and *maximum* *h*-parameter values are given, we should determine the *geometric average* of the two values. Thus the values that we would use in the analysis of circuit are found as under :

$$h_{ie} = \sqrt{h_{ie\ (min)} \times h_{ie\ (max)}}$$

$$= \sqrt{(600\ \Omega)\ (800\ \Omega)} = 693\Omega$$

$$h_{fe} = \sqrt{h_{fe\ (min)} \times h_{fe\ (max)}}$$

$$= \sqrt{(110)\ (140)} = 124$$

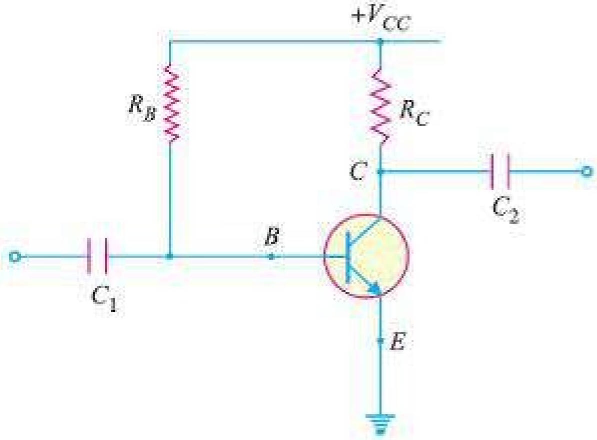
Voltage gain, $A_v = \dfrac{h_{fe}\, r_L}{h_{ie}} = \dfrac{(124)\ (460)}{693} = \mathbf{82.3}$

Determination of Transistor h-parameters:

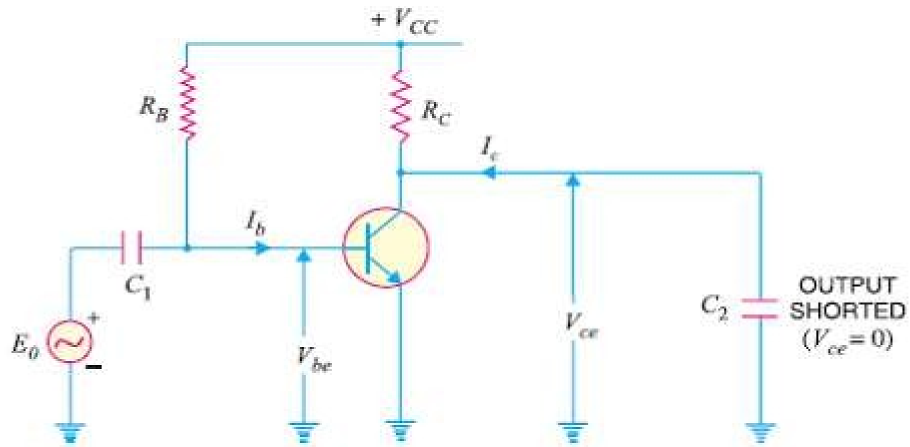
The determination of *h* parameters of a general linear circuit has already been discussed in figure To illustrate how such a procedure is carried out for a *CE* transistor amplifier, consider the circuit of figure The R.M.S. values will be considered in the discussion. Using standard transistor nomenclature :

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \quad ...(i)$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \quad ...(ii)$$



(i) **Determination of h_{fe} and h_{ie}.** In order to determine these parameters, the output is a.c. short circuited as shown in Fig. This is accomplished by making the capacitance of C_2 deliberately large. The result is that changing component of collector current flows through C_2 instead of R_C and a.c. voltage developed across C_2 is zero *i.e.* *$V_{ce} = 0$.



Substituting $V_{ce} = 0$ in equations (*i*) and (*ii*) above, we get,

$$V_{be} = h_{ie} I_b + h_{re} \times 0$$

$$I_c = h_{fe} I_b + h_{oe} \times 0$$

$$\therefore \qquad h_{fe} = \frac{I_c}{I_b} \quad \text{for} \quad V_{ce} = 0$$

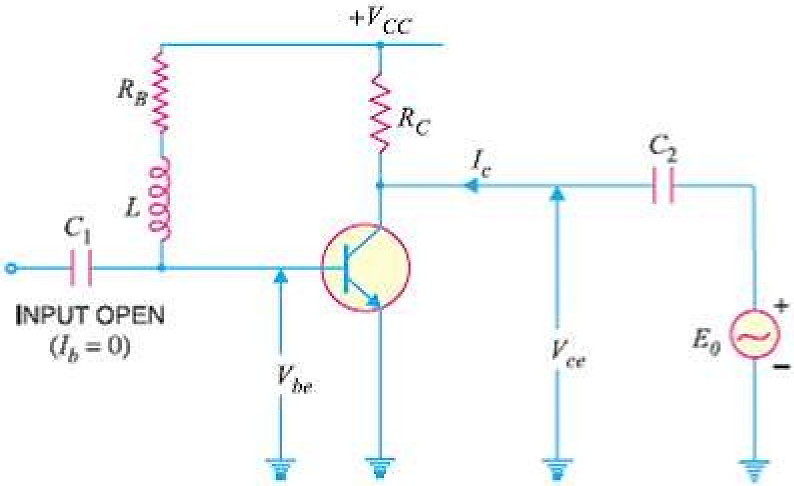
and

$$h_{ie} = \frac{V_{be}}{I_b} \quad \text{for } V_{ce} = 0$$

Note that I_c and I_b are the a.c. R.M.S. collector and base currents respectively. Also V_{be} is the a.c. R.M.S. base-emitter voltage.

* Note that setting $V_{ce} = 0$ does not mean that V_{CE} (the d.c. collector-emitter voltage) is zero. Only a.c. output is short-circuited.

(ii) Determination of h_{re} and h_{oe}. In order to determine these two parameters, the input is a.c. open-circuited, a signal generator is applied across the output and resulting V_{be}, V_{ce} and I_c are measured. This is illustrated in Fig (ii). A large inductor L is connected in series with R_B. Since the d.c. resistance of inductor is very small, it does not disturb the operating point. Again, a.c. current cannot flow through R_B because of large reactance of inductor. Further, the voltmeter used to measure V_{be} has a high input impedance and hence there are no paths connected to the base with any appreciable a.c. current. This means that base is *effectively a.c. open-circuited *i.e.* $I_b = 0$.



Substituting $I_b = 0$ in equations (i) and (ii), we get,

$$V_{be} = h_{ie} \times 0 + h_{re} V_{ce}$$

$$I_c = h_{fe} \times 0 + h_{oe} V_{ce}$$

$\therefore$ $$h_{re} = \frac{V_{be}}{V_{ce}} \text{ for } I_b = 0$$

and $$h_{oe} = \frac{I_c}{V_{ce}} \text{ for } I_b = 0$$

Example *The following quantities are measured in a CE amplifier circuit :*

(a) With output a.c. short-circuited (i.e. $V_{ce} = 0$)

$$I_b = 10\ \mu A;\ I_c = 1\ mA;\ V_{be} = 10\ mV$$

(b) With input a.c. open-circuited (i.e. $I_b = 0$)

$$V_{be} = 0.65\ mV;\ I_c = 60\ \mu A;\ V_{ce} = 1\ V$$

Determine all the four h parameters.

Solution.

$$h_{ie} = \frac{V_{be}}{I_b} = \frac{10 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{1000\ \Omega}$$

$$h_{fe} = \frac{I_c}{I_b} = \frac{1 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{100}$$

$$h_{re} = \frac{V_{be}}{V_{ce}} = \frac{0.65 \times 10^{-3}}{1} = \mathbf{0.65 \times 10^{-3}}$$

* How effectively the base is a.c. open-circuited depends upon the reactance L and the input impedance of the voltmeter used to measure V_{be}.

$$h_{oe} = \frac{I_c}{V_{ce}} = \frac{60 \times 10^{-6}}{1} = 60\,\mu\text{mho}$$

Limitations of h-parameters:

The *h* parameter approach provides accurate information regarding the current gain, voltage gain, input impedance and output impedance of a transistor amplifier. However, there are two major limitations on the use of these parameters.

(*i*) It is very difficult to get the exact values of *h* parameters for a particular transistor. It is because these parameters are subject to considerable variation—unit to unit variation, variation due to change in temperature and variation due to change in operating point. In predicting an amplifier performance, care must be taken to use *h* parameter values that are correct for the operating point being considered.

(*ii*) The *h* parameter approach gives correct answers for small a.c. signals only. It is because a transistor behaves as a linear device for small signals only.

Comparison of transistor amplifiers:

Transistor CB (Common Base) configuration:

It is transistor circuit in which base is kept common to the input and output circuits.
Characteristics:

- It has low input impedance (on the order of 50 to 500 Ohms).
- It has high output impedance (on the order of 1 to 10 Mega Ohms).
- Current gain(alpha) is less than unity.

Transistor CE (Common Emitter) configuration:

It is transistor circuit in which emitter is kept common to both input and output circuits.
Characteristics (applications):

- It has high input impedance (on the order of 500 to 5000 Ohms).
- It has low output impedance (on the order of 50 to 500 Kilo Ohms).
- Current gain (Beta) is 98.
- Power gain is upto 37 dB.
- Output is 180 degree out of phase.

Transistor CC (Common Collector) configuration:

It is transistor circuit in which collector is kept common to both input and output circuits. It is also called as emitter follower.
Characteristics:

- It has high input impedance (on the order of about 150 to 600 Kilo Ohms).
- It has low output impedance (on the order of about 100 to 1000 Ohms).
- Current gain (Beta) is about 99.
- Voltage and power gain is equal to or less than one.

Following table summarizes important points about CB,CE,CC transistor configurations.

Parameter	Common Base	Common Emitter	Common Collector
Voltage Gain	High, Same as CE	High	Less than Unity
Current Gain	Less than Unity	High	High
Power Gain	Moderate	High	Moderate

Phase inversion	No	Yes	No
Input Impedance	Low (50 Ohm)	Moderate (1 KOhm)	High (300 KOhm)
Output Impedance	High (1 M Ohm)	Moderate (50 K)	Low (300 Ohm)

<u>Generalized analysis of small signal model of FET:</u>

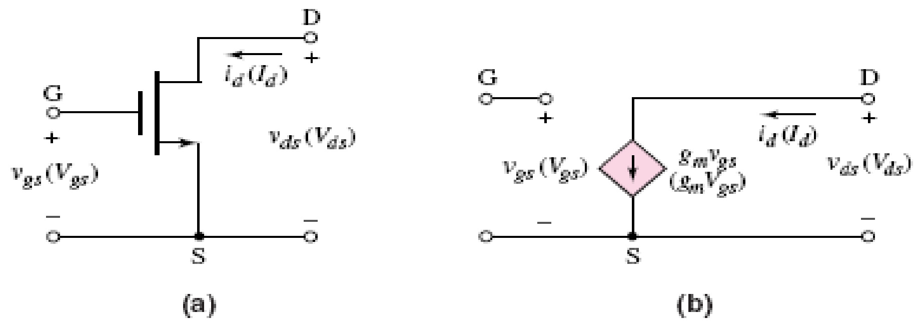


Fig. (a) CS Amplifier and (b) Small Signal Model

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has a much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor β (beta), the FET has a transconductance factor, g_m.

While the common-source configuration is the most popular, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity. While the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

Analysis of CG, CS and CD amplifiers:

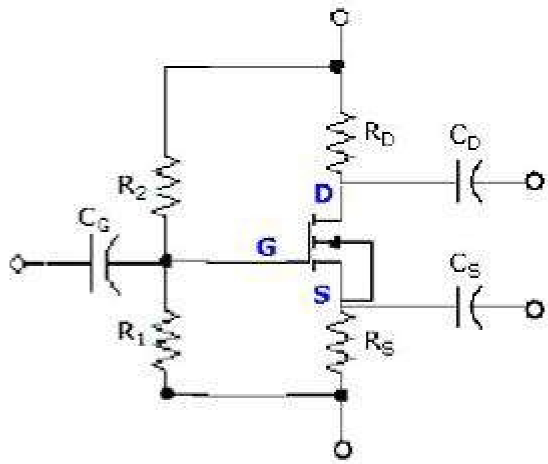


Figure 5.1: FET Amplifier

Just as there were four basic configurations for a single stage BJT amplifier (CE, ER, CC, and CB), there are four basic configurations for a single stage FET amplifier. With respect to the figure to the right (a modified version of Figure 6.31 in your text), these configurations may be defined as follows:

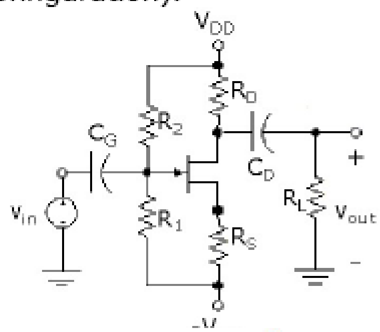
- In the **common source (CS)** configuration, the ac input is applied at C_G, the ac output is taken at C_D and C_S is connected to a dc voltage source or ground. This is analogous to the common-emitter configuration of the BJT. Note the distinction between CS (the configuration) and C_S (the capacitor) – don't let this confuse you.
- In the **source resistor (SR)** configuration, the ac input is applied at C_G, the ac output is taken at C_D and C_S is omitted. This is analogous to the emitter-resistor configuration of the BJT.
- In the **common gate (CG)** configuration, the ac input is applied at C_S, the ac output is taken at C_D and C_G is connected to a dc voltage course or ground. Sometimes in the CG configuration, C_G is omitted and the gate is connected directly to a dc voltage source. The CG is analogous to the common base configuration for the BJT, although it is seldom used. Note the distinction between CG (the configuration) and C_G (the capacitor) – don't let this confuse you.
- In the **source follower (SF)** configuration, the ac input is applied at C_G, the ac output is taken at C_S and the drain is either connected to a dc voltage supply (with or without C_D). This is also called the **common drain (CD)** and is analogous to the common collector (a.k.a. emitter follower) configuration for the BJT.

Although the circuit above shows an enhancement NMOS, these configurations are valid for all JFETs and MOSFETs discussed. Also, keep in mind that the circuit capacitors serve as coupling or bypass, depending on the configuration, and are assumed to be large enough to act as open circuits for dc and short circuits for the frequency range of interest.

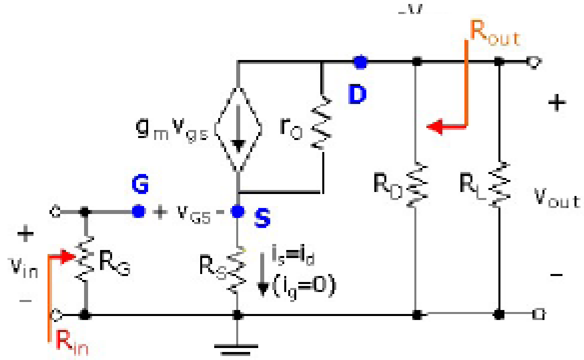
The CS and SR Amplifier

To avoid duplicate derivations, the following discussion will focus on the source resistor configuration. From the source resistor results, we can obtain expressions for the common source configuration by setting $R_S=0$ in all equations (since R_S is bypassed by C_S in the CS configuration).

The SR amplifier circuit is shown to the right (based on Figure 6.33a of your text). As defined above, the ac input is applied at C_G and the ac output is taken at C_D. The CS amplifier circuit is exactly the same with the addition of C_S, which is connected to the dc voltage source or ground.



The ac small signal model for the source resistor configuration is shown to the right and is a modified version of Figure 6.33b in your text. I have explicitly



shown the device output resistance, r_O, in this circuit for the sake of completeness. However, as we found for the BJT (and your author assumes), this output resistance is usually much larger than the resistances it is in parallel with and may be neglected. By following the same strategy as we used for the emitter-resistor configuration, R_{out} for the source resistor configuration is found to be

$$R_{out} = [r_O + R_S(1+g_m r_O)] \,\|\, R_D .$$

Note that if $r_O >> R_S$ and $r_O >> R_D$, this may be simplified to

$$R_{out} \cong R_D .$$

By inspection, the input resistance of the SR circuit is

$$R_{in} = R_G = R_1 \,\|\, R_2 .$$

To calculate the voltage gain, we need expressions for v_{in} and v_{out} in terms of circuit components. The following presentation is slightly different from your text's derivation, but we get to the same place.

To solve for v_{in}, we write a KVL equation around the gate loop:

$$v_{in} = v_{gs} + i_d R_S = v_{gs} + g_m v_{gs} R_S = v_{gs}(1+g_m R_S) . \qquad \text{(Equation 6.42)}$$

The output voltage may be expressed as

$$v_{out} = -i_d (R_D \parallel R_L) = -g_m v_{gs} (R_D \parallel R_L).$$

Calculating the voltage gain $A_V = v_{out}/v_{in}$, we get

$$A_V = \frac{-g_m (R_D \parallel R_L)}{(1+g_m R_S)} = \frac{-(R_D \parallel R_L)}{R_S + 1/g_m}. \qquad \text{(Equation 6.43)}$$

Finally, either by using the gain impedance formula or by using a current divider to define the output current (the current through the load) and defining current gain in the usual way, we get

$$A_i = \frac{-R_G}{R_S + 1/g_m} \frac{R_D}{R_D + R_L}. \qquad \text{(Equation 6.45)}$$

As mentioned earlier, the relevant equations for the CS configuration may be found by modifying what we've just derived. Specifically, when $R_S=0$, the common source configuration results are:

$$R_{out} = r_O \,||\, R_D \cong R_D \quad \text{if} \quad r_O >> R_D$$

$$R_{in} = R_G = R_1 \parallel R_2$$

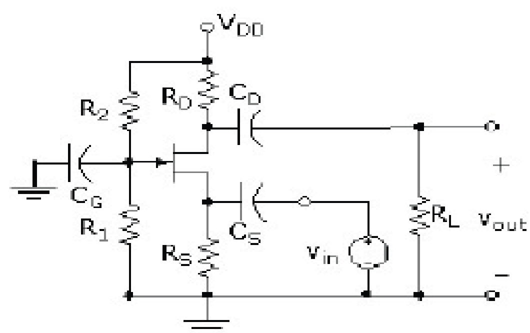
$$A_V = -g_m (R_D \parallel R_L)$$

$$A_i = \frac{-g_m R_G R_D}{R_D + R_L}$$

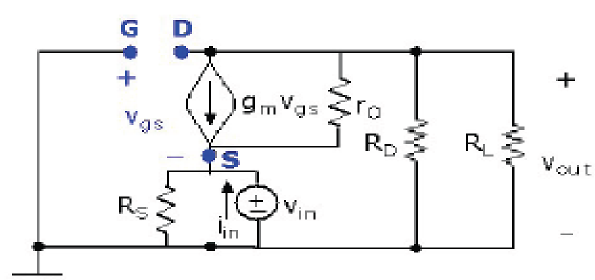
Finally, note that the voltage and current gains for both the CS and SR configurations are negative, indicating a 180° phase shift between input and output (just like we had for the BJT CE and ER).

The CG Amplifier

A modified version of Figure 6.37a is shown to the right. *In this schematic of a common gate amplifier, I have removed the source resistance R_{source} and applied v_{in} directly. What I'm trying to do here folks is maintain consistency in the notation – when we use v_{in} it is applied directly to the amplifier. An alternate representation is the derivation of v_{in} through a voltage divider relationship from a source voltage and resistance (v_{source} and R_{source}).* As defined in the introductory comments of this section, the ac input is applied at C_S, the ac output is taken at C_D and C_G is connected to ground.



The ac small signal model for the CG amplifier is shown to the right (Note that the illustration given in Figure 6.37b of your text is incorrect.).



To derive the output resistance, we follow the same procedure as above… with the same results. Therefore, for the CG amplifier:

$$R_{out} = [r_O + R_S(1+g_m r_O)] \| R_D \cong R_D \quad if \quad r_O >> R_D.$$

To derive the input resistance, we need to use the figure above. Using KCL, the current through R_S may be expressed as (note that R_S is in parallel with v_{in} so it carries the same voltage and that the gate-to-source voltage is the same magnitude, but opposite polarity, as v_{in}):

$$i_{in} = \frac{v_{in}}{R_S} - g_m v_{gs} = \frac{v_{in}}{R_S} + g_m v_{in} = v_{in}\left(\frac{1}{R_S} + g_m\right). \quad \text{(Equations 6.46 \& 6.47)}$$

Using this result, we can calculate the input resistance as

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{1/R_S + g_m} = R_S \| \frac{1}{g_m}. \quad \text{(Equation 6.48)}$$

Using $v_{out}=-g_m v_{gs}(R_D||R_L)=g_m v_{in}(R_D||R_L||r_O)$, the voltage gain for the CG amplifier is given by:

$$A_V = \frac{g_m v_{in}(R_D \| R_L \| r_O)}{v_{in}} \cong g_m(R_D \| R_L) \quad if \quad r_O >> R_D, R_L. \quad \text{(Equation 6.49)}$$

Note that the gain for the CG is the same as for the CS, without the negative sign. This means that the two configurations will provide the same voltage gain, but the CG output will be in phase with the input.

The current gain of the CG amplifier is given by:

$$A_I = \frac{(R_D \| R_L \| r_O)}{R_L} \frac{R_S}{R_S + 1/g_m} \cong \frac{R_D}{R_D + R_L} \frac{R_S}{R_S + 1/g_m} \quad if \quad r_O >> R_D, R_L \quad \text{(Equation 6.50)}$$

The CD (SF) Amplifier

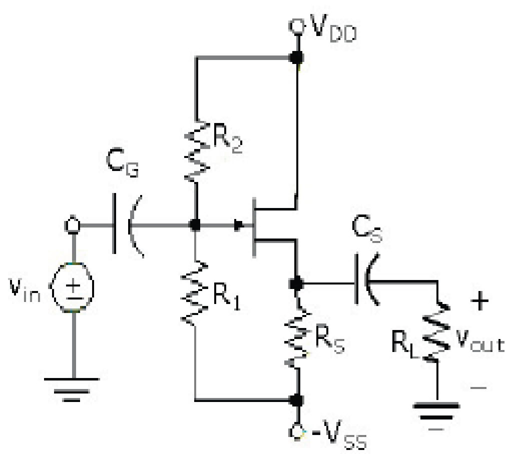
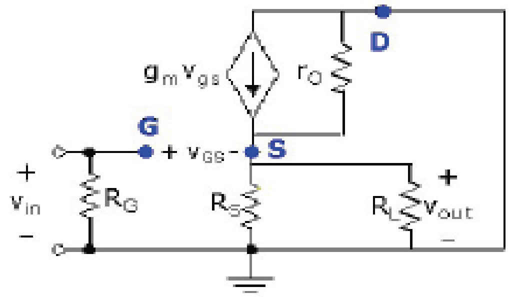


Figure 6.39a (corrected and reproduced to the right) shows the schematic of a single-stage common drain (CD)/source follower (SF) circuit. As defined earlier, the ac input is applied at C_G, the ac output is taken at C_S and the drain is either connected to a dc voltage supply

or the drain resistor is bypassed with capacitor C_D (in this example the drain is connected to V_{DD} without C_D).

The ac small signal model for the CD (SF) amplifier is shown in Figure 6.39b and to the right.



Following the procedure used several times (this time we'll put a test voltage source in the source-ground leg and set $v_{in}=0$ so that $v_{gs}=-v_{test}$) an expression for the output resistance may be obtained:

$$i_{test} = \frac{v_{test}}{R_S} + g_m v_{test} = v_{test}\left(\frac{1}{R_S} + g_m\right), \text{ and}$$

$$R_{out} = \frac{v_{test}}{i_{test}} = \frac{1}{1/R_S + g_m} = R_S \parallel \frac{1}{g_m}. \qquad \text{(Equation 6.57)}$$

By inspection, the input resistance of the common drain amplifier is

$$R_{in} = R_G = R_1 \parallel R_2.$$

To solve for the voltage gain, we need expressions for v_{in} and v_{out} in terms of circuit components. By inspection, $v_{out}=g_m v_{gs}(R_S \| R_L)$. To obtain the expression for v_{in}, write the KVL equation around the gate-source loop:

$$v_{in} = v_{gs} + (R_S \parallel R_L) g_m v_{gs} = v_{gs}[1 + g_m(R_S \parallel R_L)].$$

Calculating the voltage gain as the ratio of output voltage to input voltage:

$$A_V = \frac{g_m(R_S \parallel R_L)}{[1 + g_m(R_S \parallel R_L)]} = \frac{R_S \parallel R_L}{(R_S \parallel R_L) + 1/g_m}. \qquad \text{(Equation 6.54)}$$

And...finally, (the last one!) the current gain for the CD/SF configuration is:

$$A_i = \frac{R_G R_S}{(R_S + R_L)[(R_S \parallel R_L) + 1/g_m]}. \qquad \text{(Equation 6.55)}$$

Comparison of FET amplifiers:

The following table presents a summary of our discussions in this section. Note that these designations are with respect to the other FET configurations; for example, the CS is shown to have a high voltage gain, but it is still significantly lower than achievable with a BJT amplifier.

Amplifier Configuration	Z_{in}	Z_{out}	A_v	A_i
Ideal	∞	0	∞	∞
Common Source (CS)	High	High	High	High
Source Resistor (SR)	High	High	Medium	Medium
Common Gate (CG)	Low	Low	High	Low (~1)
Source Follower (SF)/ Common Drain (CD)	High	Low	Low (~1)	High