SVR ENGINEERING COLLEGE

Approved by AICTE & Permanently Affiliated to JNTUA

Ayyalurmetta, Nandyal – 518503. Website: www.svrec.ac.in

Department of Electronics and Communication Engineering

(19A04302P) ELECTRONIC DEVICES AND CIRCUITS LAB

II B. Tech (ECE) I Semester 2020-21

STUDENT NAME	
ROLL NO.	
SECTION	

SVR ENGINEERING COLLEGE

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DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

ACADEMIC YEAR: 2020-21

This is to certify that the bonafide record work done by Mr./Ms._____ bearing H.T.NO. _____ of II B. Tech I Semester in the

Electronic devices and circuits laboratory.

Faculty In-Charge **Head of the Department**

SYLLABUS

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

B.Tech –II-I Sem 19A04302P ELECTRONIC DEVICES AND CIRCUITS LAB

LIST OF EXPERIMENTS: Branch : For ECE only R19

1. Verification of Volt-Ampere characteristics of a PN junction diode and find static, dynamic and reverse resistances of the diode from the graphs obtained.

2. Design a full wave rectifier for the given specifications with and without filters, and verify the given specifications experimentally. Vary the load and find ripple factor. Draw suitable graphs.

3. Verify various clipping and clamper circuits using PN junction diode and draw the suitable graphs.

4. Design a Zener diode based voltage regulator against variations of supply and load. Verify the same from the experiment.

5. Study and draw the output and transfer characteristics of MOSFET (Enhance mode) in Common Source Configuration experimentally. Find Threshold voltage (v_T), g_m, & K from the graphs.

6. Study and draw the output and transfer characteristics of MOSFET (Depletion mode) or JFET in Common Source Configuration experimentally. Find I_{DSS}, gm, & V_P from the graphs.

7. Verification of the input and output characteristics of BJT in Common Emitter configuration experimentally and find required h –parameters from the graphs.

8. Study and draw the input and output characteristics of BJT in Common Base configuration experimentally, and determine required h –parameters from the graphs.

9. Verify the Volt Ampere characteristics of SCR experimentally and determine holding current and break over voltage from the graph.

10. Study and draw the Volt Ampere characteristics of UJT and determine η, I_P, Iv, V_P , & Vv from the experiment.

11. Design and analysis of voltage-divider bias/self bias circuit using BJT.

12. Design and analysis of voltage-divider bias/self bias circuit using JFET.

13. Design and analysis of self bias circuit using MOSFET.

14. Design a suitable circuit for switch using CMOSFET/JFET/BJT.

Note: All the experiments shall be implemented using both Hardware and Software. Student has to perform minimum of any 12 experiments.

ECE DEPT VISION & MISSION PEOs and PSOs

Vision

To produce highly skilled, creative and competitive Electronics and Communication Engineers to meet the emergingneeds of the society.

Mission

- Impart core knowledge and necessary skills in Electronics and Communication Engineering throughinnovative teaching and learning.
- Inculcate critical thinking, ethics, lifelong learning and creativity needed for industry and society
- Cultivate the students with all-round competencies, for career, higher education and self-employability
-

I. PROGRAMME EDUCATIONAL OBJECTIVES (PEOS)

PEO1: Graduates apply their knowledge of mathematics and science to identify, analyze and solve problems in the field of Electronics and develop sophisticated communication systems.

PEO2: Graduates embody a commitment to professional ethics, diversity and social awareness in theirprofessional career.

PEO3: Graduates exhibit a desire for life-long learning through technical training and professional activities.

II. PROGRAM SPECIFIC OUTCOMES (PSOS)

PSO1: Apply the fundamental concepts of electronics and communication engineering to design a variety of components and systems for applications including signal processing, image processing, communication, networking, embedded systems, VLSI and control system

PSO2: Select and apply cutting-edge engineering hardware and software tools to solve complex Electronics and Communication Engineering problems.

III. PROGRAMME OUTCOMES (PO'S)

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and anengineering specialization to the solution of complex engineering problems.

2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, andin multidisciplinary settings.

10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects andin multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

IV. COURSE OBJECTIVES

- To review analysis & design of single stage amplifiers using BJT & MOSFETs at low andhigh frequencies.
- To understand the characteristics of Differential amplifiers, feedback and poweramplifiers.
- To examine the response of tuned amplifiers and multi-vibrators
- To categorize different oscillator circuits based on the application
- To design the electronic circuits for the given specifications and for a given application.

V. COURSE OUTCOMES

After the completion of the course students will be able to

Course Outcomes	Course Outcome statements	BTL
CO1	Understand the basic characteristics and applications of basic electronicdevices.	L1
CO2	Observe the characteristics of electronic devices by plottinggraphs	L2
CO3	Analyze the Characteristics of UJT, BJT, FET, and SCR	L3
CO4	Design FET based amplifier circuits/BJT based amplifiers forthe given specifications.	L4
CO5	Simulate all circuits in PSPICE /Multisim.	L5

VI. COURSE MAPPING WITH PO'S AND PEO'S

Course Title	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
Electronic Circuit Analysis Lab	2.4	2.6	2.2	2.4	2.6	2.4	1.8	1.8	2.4	2.4	2.2	2.8	2.8	2.6

VII. MAPPING OF COURSE OUTCOMES WITH PEO'S AND PO'S

Course Title	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	2	3	2	2	3	2	2	1	3	3	3	3	3	3
CO2	3	2	3	2	2	2	1	2	3	2	3	2	3	3
CO3	2	3	2	3	2	3	2	2	2	1	1	3	2	2
CO4	2	2	2	2	3	2	1	2	2	3	2	3	3	2
CO5	3	3	2	3	3	3	3	2	2	3	2	3	3	3

LABORATORY INSTRUCTIONS

1. While entering the Laboratory, the students should follow the dress code. (Wear shoes and White apron,Female Students should tie their hair back).

2. The students should bring their observation book, record, calculator, necessary stationery items and graphsheets if any for the lab classes without which the students will not be allowed for doing the experiment.

3. All the Equipment and components should be handled with utmost care. Any breakage or damage will becharged.

4. If any damage or breakage is noticed, it should be reported to the concerned in charge immediately.

5. The theoretical calculations and the updated register values should be noted down in the observation bookand should be corrected by the lab in-charge on the same day of the laboratory session.

6. Each experiment should be written in the record note book only after getting signature from the lab in-charge in the observation notebook.

7. Record book must be submitted in the successive lab session after completion of experiment.

8. 100% attendance should be maintained for the laboratory classes.

Precautions.

1. Check the connections before giving the supply.
2. Observations should be done carefully.

INDEX

Max. Marks per each Experiment : 5

Exp. No. 1 **Date :**

PN JUNCTION DIODE CHARACTERISTICS

AIM :

1). To study the V-I characteristics of the PN junction diode using Silicon diode using Hardware and Software

2). To obtain the Static and Dynamic resistances in both biases.

APPARATUS :

1). Voltmeters :	a). (0 – 2)V	Digital / Analog	DC Type ----- 1 No.
	b). (0 – 50)V	Digital / Analog	DC Type ----- 1 No
2). Ammeters :	a). (0 – 50)mA	Digital / Analog	DC Type ----- 1 No.
	b). (0 – 2000)µA	Digital only	DC Type ----- 1 No.
3). Regulated Power Supply (RPS) :	(0-30)V, 1A	Dual channel,	----- 1 No.
4). Bread board			----- 1 No.
5). Connecting wires :			----- A few Nos.
6). System with Multisim Software :			------ 1 No.

COMPONENTS :

1). PN Junction Diode Silicon (Si) 1N 4007---------- 1 No.
2). Carbon fixed resistor 560 Ω , ½ W---------- 1 No.

THEORY :

Definition: A p-n junction is an interface or a boundary between two semiconductor material types, namely the p-type and the n-type, inside a semiconductor. The p-side or the positive side of the semiconductor has an excess of holes and the n-side or the negative side has an excess of electrons.

A PN Junction Diode is one of the simplest semiconductor devices around, and which has the characteristic of passing current in only one direction only. ... By applying a negative voltage (reverse bias) results in the free charges being pulled away from the junction resulting in the depletion layer width being increased.

In a standard diode, forward biasing occurs when the voltage across a diode permits the natural flow of current, whereas reverse biasing denotes a voltage across the diode in the opposite direction

Depletion region or depletion layer is a region in a P-N junction diode where no mobile charge carriers are present. Depletion layer acts like a barrier that opposes the flow of electrons from n-side and holes from p-side.

The ideal diode equation is very useful as a formula for current as a function of voltage. However, at times the inverse relation may be more useful; if the ideal diode equation is inverted and solved for voltage as a function of current, we find: $v(i)=\eta V_T \ln[(iI_S)+1]$.

CIRCUIT DIAGRAMS :

A). Forward bias using silicon (Si) diode: **B). Reverse bias using silicon (Si) diode :**

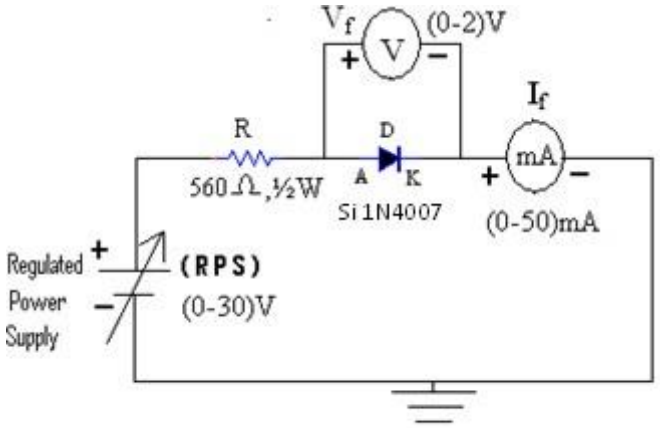


Figure: Circuit diagram of PN junction diode in forward bias using Silicon(Si) diode

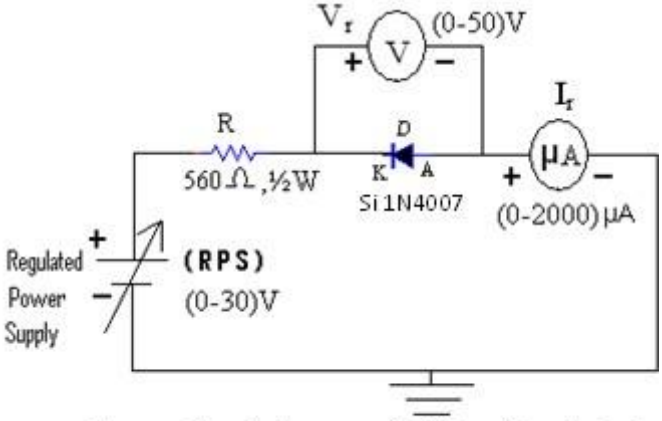


Figure: Circuit diagram of PN junction diode in reverse bias using Silicon(Si) diode

PROCEDURE :

A). Forward bias using silicon (Si) diode:

1). Connected the circuit as shown in the circuit diagrams.
2). Connected the positive terminal of the RPS to the Anode(A), negative terminal of the RPS to the Cathode(C) of the dioderespectively.
3). Then Switched ON the RPS and all themeters.
4). Varied the supply voltage (RPS voltage) in steps i.e. 0V, 0.2V, 0.4V, 0.6V, 0.8V, 1V, 5V, 10V, 15V,20V, 25V, 30V
5). After completion of readings keep the RPS voltage at 0V immediately.
6). Switched OFF the RPS and all the meters.
7). Plotted the graph between *forward voltage(V_f)*on X-axis and *forward current (I_f)*on Y- axis.
8). Calculated the *static resistance* and *dynamic resistance* from the graph by using the formulas given under the heading of parameters.
9). We did the same experiment using mul tisim software and noted down the corresponding readings in the tabular form and compared those values with the readings of Hardware.

A). Reverse bias using silicon (Si) diode

1). Connected the circuit as shown in the circuit diagrams.
2). Connected the positive terminal of the RPS to the Cathode(C), negative terminal of the RPS to the Anode(A) of the diode respectively.
3). Then Switched ON the RPS and all the meters.
4). Varied the supply voltage (RPS voltage) in steps i.e. 0V, 1V, 5V, 10V, 15V, 20V, 25V, 30V
5). After completion of readings keep the RPS voltage at 0V immediately.
6). Switched OFF the RPS and all the meters.
7). Plotted the graph between *reverse voltage (V_r)* on X-axis and *reverse current (I_r)*on Y- axis.
8). Calculated the *static resistance* and *dynamic resistance* from the graph by using the formulas given under the heading of parameters.
9). We did the same experiment using multisim software and noted down the corresponding readings in the tabular form and compared those values with the readings of Hardware.

TABULAR COLOUMNS :

A). Forward bias using silicon (Si) diode :

Using Hardware : Using Multisim software :

Sl. No.	Supply/RPS Voltage In Volts	Frward Voltage (V_f) In Volts	Forward Current (I_f) In mA		Reverse Voltage (V_r) In Volts	Reverse Current (I_r) In µA
01	0.00					
02	0.20					
03	0.40					
04	0.60					
05	0.80					
06	1.00					
07	5.00					
08	10.00					
09	15.00					
10	20.00					
11	25.00					
12	30.00					

B). Reverse bias Silicon diode :

Using Hardware : Using Multisim software :

Sl. No.	Supply/RPS Voltage In Volts	Reverse Voltage (V_f) In Volts	Reverse Current (I_f) In mA		Reverse Voltage (V_r) In Volts	Reverse Current (I_r) In µA
01	0.00					
02	1.00					
03	5.00					
04	10.00					
05	15.00					
06	20.00					
07	25.00					
08	30.00					

EXPECTED GRAPHS :

A). Forward bias using silicon (Si) diode:

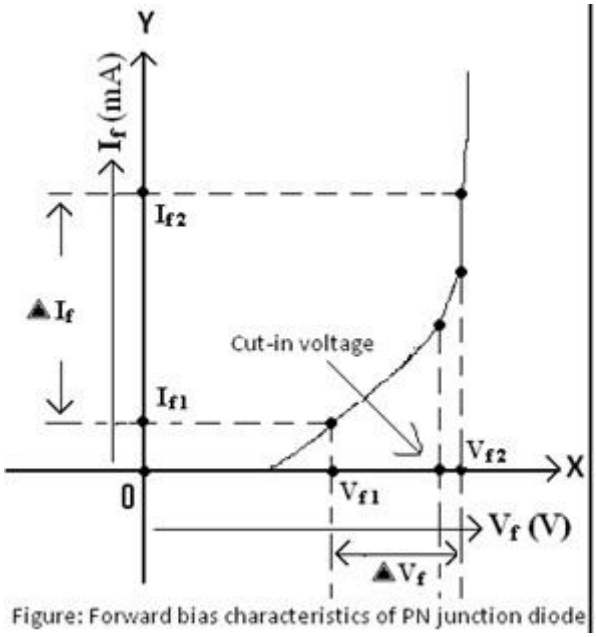


Figure: Forward bias characteristics of PN junction diode

A). Reverse bias using silicon (Si) diode:

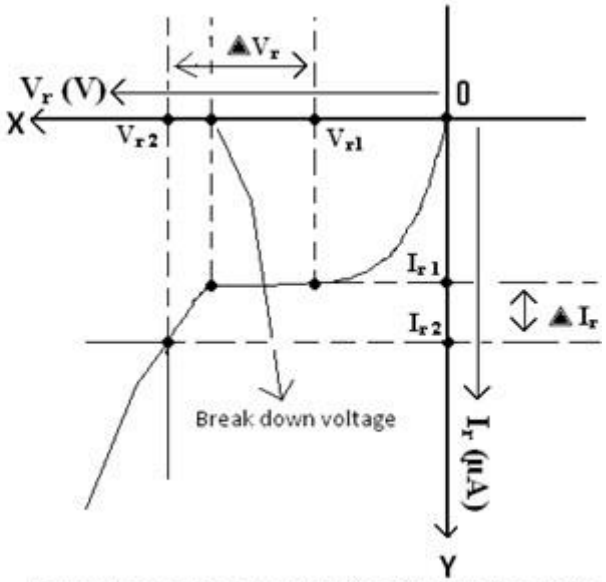


Figure: Reverse bias characteristics of PN junction diode

C). Forward bias using germanium (Ge)

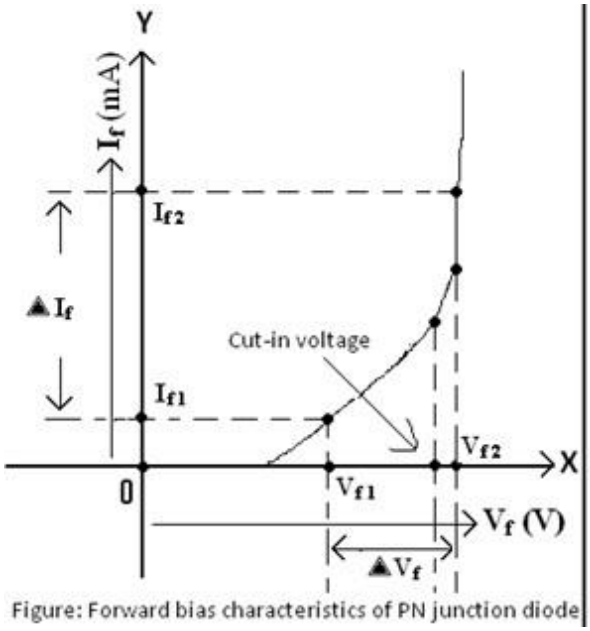


Figure: Forward bias characteristics of PN junction diode

D). Reverse bias using germanium (Ge) diode:

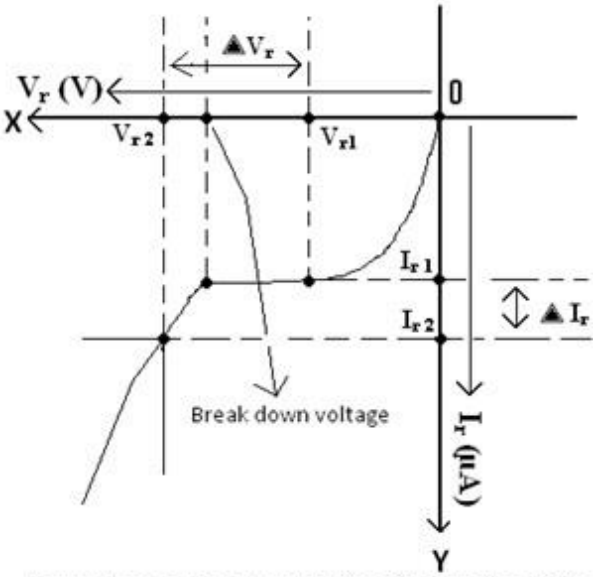


Figure: Reverse bias characteristics of PN junction diode

PARAMETERS :

A). Forward bias using silicon (Si) diode :

1). Static resistance :V_f/I_f =

2). Dynamic resistance :$\blacktriangle V_f / I_f$ =

B). Reverse bias using silicon (Si) diode:

1). Static resistance : V_r/ I_r =

2). Dynamic resistance : $\blacktriangle V_r / I_r$ =

RESULT :

We studied the V-I characteristics of *PN junction diode* in forward bias and reverse bias using silicon (Si) diode.

VIVA VOCE Questions:

1. What is Semi Conductor?

2. What are the Classification of materials?

3. Explain Intrinsic and Extrinsic Semiconductors.

4. Define PN Diode.

5. What is the Cut- In- Voltage of Si and Ge Diodes?

6. Mention PN Junction Diode Applications.

7. What is the Diode current equation?

8. What is the Static Resistance?

9. What is the Dynamic Resistance?

10. What are the Temperature effects on PN Junction Diode?

Exp. No. 2 Date :

FULL WAVE RECTIFIER

AIM :

1). To study the characteristics of *Full wave rectifier with an without filter* using Software & Hardware
2). To obtain the ripple factor and percentage of regulation of this same.

APPARATUS :

1). Voltmeter :	(0 – 20)V	Digital / Analog	DC Type	---------1 No
2). Ammeters :	(0 – 500)mA	Digital / Analog	DC Type	--- 1 No.
3). Digital Multi Meter (DMM)				-------- 1 No.
4). Decade Resistance Box (DRB)				-------- 1 No.
5). Cathode Ray Oscilloscope (CRO)				-------- 1 No.
6). Probes				-------- 2 No.
7). Bread board				-------- 1 No.
8). Connecting wires :				-------- A few Nos.
9). System with Multisim Software	:			------ 1 No.

COMPONENTS :

1). PN Diode 1N4007		-------- 2 No.
2). Electrolytic capacitor (Filter)	i). 100µF, 25V	-------- 1 No.
	ii). 1000µF,25V	-------- 1No.
3). Centre tapped step down transformer	12-0-12V, 500mA	------- 1 No.

THEORY :

Defination :

A full wave rectifier is defined as a rectifier that converts the complete cycle of alternating current into pulsating DC.

Working of Full Wave Rectifier :

The input AC supplied to the full wave rectifier is very high. The step-down transformer in the rectifier circuit converts the high voltage AC into low voltage AC. The anode of the centre tapped diodes is connected to the transformer's secondary winding and connected to the load resistor. During the positive half cycle of the alternating current, the top half of the secondary winding becomes positive while the second half of the secondary winding becomes negative.

During the positive half cycle, diode D_1 is forward biased as it is connected to the top of the secondary winding while diode D_2 is reverse biased as it is connected to the bottom of the secondary winding. Due to this, diode D_1 will conduct acting as a short circuit and D_2 will not conduct acting as an open circuit

During the negative half cycle, the diode D_1 is reverse biased and the diode D_2 is forward biased because the top half of the secondary circuit becomes negative and the bottom half of the circuit becomes positive. Thus in a full wave rectifiers, DC voltage is obtained for both positive and negative half cycle.

Advantages of Full Wave Rectifier

- The rectification efficiency of full wave rectifiers is double that of half wave rectifiers. The efficiency of half wave rectifiers is 40.6% while the rectification efficiency of full wave rectifiers is 81.2%.
- The ripple factor in full wave rectifiers is low hence a simple filter is required. The value of ripple factor in full wave rectifier is 0.482 while in half wave rectifier it is about 1.21.
- The output voltage and the output power obtained in full wave rectifiers are higher than that obtained using half wave rectifiers.

CIRCUIT DIAGRAMS :

A). Full wave rectifier without Filter :

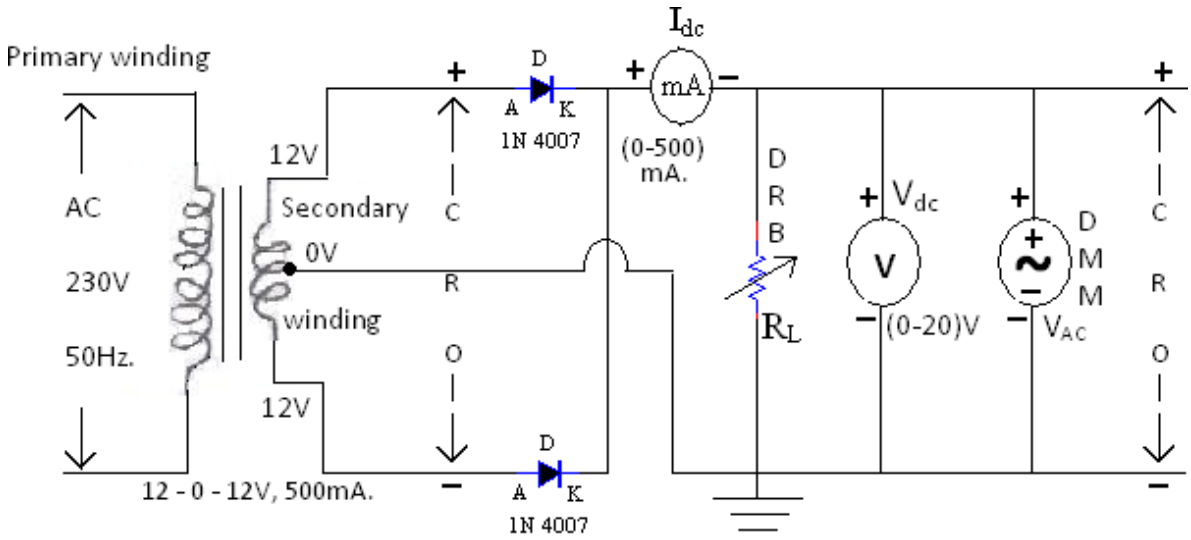


Figure: Circuit diagram of Full wave rectifier without filter

B). Full wave rectifier with 100µF & 1000µF Filter (Capacitor):

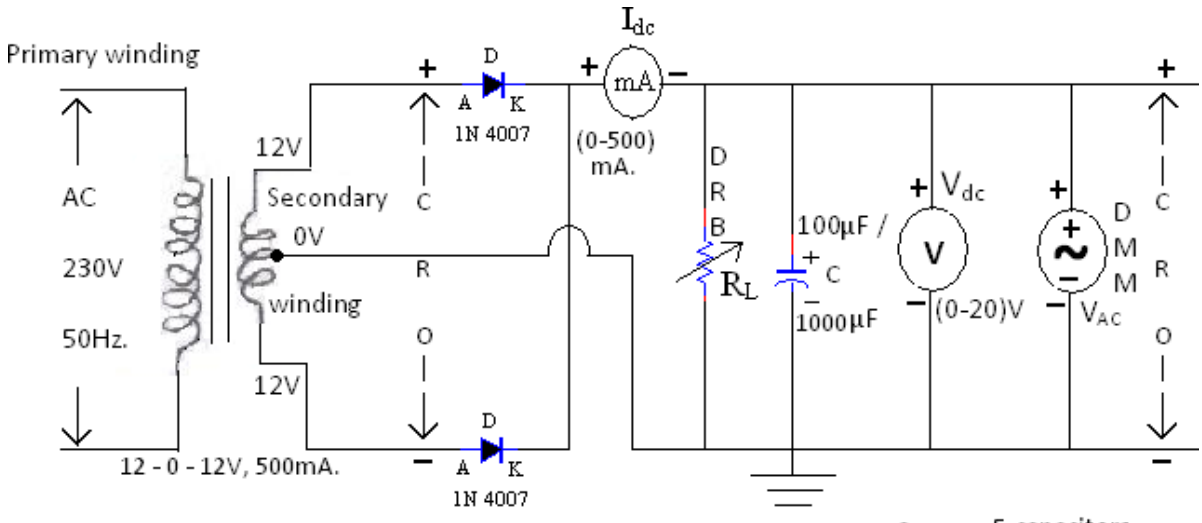


Figure: Circuit diagram of full wave rectifier with filter using 100 µF & 1000 µF capacitors

PROCEDURE :

A). Full wave rectifier without Filter :

1). Connected the circuit as shown in the circuit diagram.
2). Connected the channel1's probe of CRO across the secondary winding and channel2's probe of CRO across the output (DMM) side (as per shown in the circuit) to observe the input sine wave form and output signal respectively.
3). Removed the Decade resistance box (DRB) i.e. load resistance(R_L) from the circuit.
4). Then switched ON the transformer, and all the meters in the circuit, but don't switched ON the CRO.
5). Noted down the No load DC voltage(V_{NL}) in the given specified tabular form from the DMM.
6). After that kept the 100Ω resistance value in the DRB.
7). Now reconnected the DRB to the circuit.
8). Varied the DRB in steps of 100Ω, 500Ω, 1KΩ, 20KΩ, 40KΩ, 60KΩ ,80KΩ, 90KΩ and noted down the values of D Current (I_{dc}), DC voltage(V_{dc}), AC voltage(V_{AC}) from the corresponding meters.
9). Took care about that DRB always is not at 0Ω resistance value while taking the readings otherwise components and instruments connected in the circuit may get damage.
10). Now kept the DRB at standard resistance value of 1KΩ.
11). Then switched ON the CRO.
12). Kept the *AC/GND/DC* switch of channel1 is at *AC* position and channel2 is at *DC* position.
13). Now kept the *channel position* switch of CRO is at dual mode.
14). Plotted the input sine wave (which is at secondary side & available in channel1) and output signal (which is across DMM & available in channel2) on single graph sheet by observing in the *CRO*.
15). Now switched OFF the transformer, CRO and all the meters in the circuit.
16). Calculated the ripple factor(RF) and % of load regulation by using the formulas given below,

$$RF = V_{ac} / V_{dc} \quad \text{and \% of load regulation} = \left[\frac{V_{NL} - V_L}{V_L}\right] \times 100$$

17). Plotted the graphs as per below,
a). DC current (I_{dc}) on X-axis and Ripple factor(RF)on Y-axis.
b). DC current (I_{dc}) on X-axis and % of regulation Y- axis.
18). We did the same in the Multisim software and noted down the corresponding values in the tabular column.
19). We compared the Hardware & Software values.

B). Full wave rectifier with 100µF & 1000µF Filter (Capacitor) :

1). Connected the circuit by using 100µF filter (capacitor) as shown in the circuit diagrams.
2). Connected the channel1's probe of CRO across the secondary winding and channel2's probe of CRO across the output (DMM) side (as per shown in the circuit) to observe the input sine wave form and output signal respectively.
3). Removed the Decade resistance box (DRB) i.e. load resistance(R_L) fromthe circuit.
4). Then switched ON the transformer, and all the meters in the circuit.
5). But don't switched ON the CRO.
6). Noted down the No load DC voltage(V_{NL}) in the given specified tabular form from the DMM.
7). 7). After that kept the 100Ω resistance value in the DRB.
8). Now reconnected the DRB to the circuit.
9). Varied the DRB in steps of 100Ω, 500Ω, 1KΩ, 20KΩ, 40KΩ, 60KΩ ,80KΩ, 90KΩ and noted down the values of DC Current (I_{dc}), DC voltage(V_{dc}), AC voltage(V_{AC}) from the corresponding meters.
10). Took care about that DRB always is not at 0Ω resistance value while taking the readings otherwise components and instruments connected in the circuit may get damage.
11). Now kept the DRB at standard resistance value of 1KΩ.
12). Then switched ON the CRO.
13). Kept the *AC/GND/DC* switch of channel1 is at *AC* position and channel2 is at *DC* position.
14). Now kept the *channel position* switch of CRO is at dual mode.
15). Plotted the input sine wave (which is at secondary side & available in channel1) and output signal (which is across DMM & available in channel2) on single graph sheet by observing in the *CRO*.
16). Now switched OFF the transformer, CRO and all the meters in the circuit.
17). Then disconnected the 100µF capacitor and reconnect the 1000µF in thesame place.
18). 18). Repeated the same procedure from step 3 To step 15.
19). Calculated the ripple factor(RF) and % of load regulation for 100µF and 1000µF by using the formulas given below,

$$RF = V_{ac} / V_{dc} \quad \text{and \% of load regulation} = \left[\frac{V_{NL} - V_L}{V_L}\right] \times 100$$

20). Drawn the following 4 graphs for each time when 100µF and 1000µF capacitors are connected, (It means 4 graphs when 100µF and another 4 graphs when 1000µF capacitors are connected).
   a). DC current (I_{dc}) on X-axis and Ripple factor(RF) onY-axis.
   b). DC current (I_{dc}) on X-axis and % of regulation Y-axis.
   c). Load resistance(R_L) on X-axis and Ripple Factor (RF) on Y-axis.
   d). Load resistance(R_L) on X-axis and % of Load regulation (RF) on Y-axis.
21). We did the same in the Multisim software and noted down the corresponding values in the tabular column.
22). We compared the Hardware & Software values.

Note : We did the all above experiments in multisim software also and noted down the all the corresponding readings in the corresponding tabular columns.

TABULAR COLUMNS :

A). Full wave rectifier without Filter using Multisim software :

	No Load dc voltage (V_{NL}) = _____ In Volts.					
Sl. No.	**Load Resistance R_L Ω/KΩ**	**DC current (I_{dc}) in mA.**	**DC voltage (V_{dc} / V_L) inVolts.**	**AC voltage (V_{ac}) in Volts.**	**Ripple Factor $R_F=V_{ac}/V_{dc}$**	**% Of Regulation $=\left[\frac{V_{NL}-V_L}{V_L}\right]\times 100$**
1	100Ω					
2	500Ω					
3	1KΩ					
4	20KΩ					
5	40KΩ					
6	60KΩ					
7	80KΩ					
8	90KΩ					

B). Full wave rectifier without Filter using Hardware :

No Load dc voltage (V_{NL}) = In Volts.

Sl. No	**Load Resistance R_L Ω/KΩ**	**DC current (I_{dc}) i n mA.**	**DC voltage (V_{dc} / V_L) inVolts.**	**AC voltage (V_{ac}) in Volts.**	**Ripple Factor $R_F=V_{ac}/V_{dc}$**	**% Of Regulation $=\left[\frac{V_{NL}-V_L}{V_L}\right]\times 100$**
1	100Ω					
2	500Ω					
3	1KΩ					
4	20KΩ					
5	40KΩ					
6	60KΩ					
7	80KΩ					
8	90KΩ					

C). Full wave rectifier with 100μF capacitor filter using Multisim software :

No Load dc voltage (V_{NL}) =_____In volts.

Sl. No.	Load Resistance (R_L) In Ω/KΩ	DC current (I_{dc}) in mA.	DC Voltage (V_{dc} / V_L) in Volts.	AC voltage (V_{ac}) in Volts.	Theoretical Ripple Factor (R_F) = $\frac{1}{4\sqrt{3}(F \times C \times R_L)}$	Practical Ripple Factor (R_F)= V_{ac}/V_{dc}	% Of Regulation $=\left[\frac{V_{NL}-V_L}{V_L}\right]\times 100$
1	100Ω						
2	500Ω						
3	1KΩ						
4	20KΩ						
5	40KΩ						
6	60KΩ						
7	80KΩ						
8	90KΩ						

D). Full wave rectifier with 100μF capacitor filter using Hardware :

No Load dc voltage (V_{NL}) =_____In volts.

Sl. No.	Load Resistance (R_L) In Ω/KΩ	DC current (I_{dc}) in mA.	DC Voltage (V_{dc} / V_L) in Volts.	AC voltage (V_{ac}) in Volts.	Theoretical Ripple Factor (R_F) = $\frac{1}{4\sqrt{3}(F \times C \times R_L)}$	Practical Ripple Factor (R_F)= V_{ac}/V_{dc}	% Of Regulation $=\left[\frac{V_{NL}-V_L}{V_L}\right]\times 100$
1	100Ω						
2	500Ω						
3	1KΩ						
4	20KΩ						
5	40KΩ						
6	60KΩ						
7	80KΩ						
8	90KΩ						

E). Full wave rectifier with 1000μF capacitor filter using Multisim software :

No Load dc voltage (V_{NL}) =_____In volts.

Sl. No.	Load Resistance (R_L) In Ω/KΩ	DC current (I_{dc}) in mA.	DC Voltage (V_{dc} / V_L) in Volts.	AC voltage (V_{ac}) in Volts.	Theoretical Ripple Factor (R_F) = $\frac{1}{4\sqrt{3}(F \times C \times R_L)}$	Practical Ripple Factor (R_F)= V_{ac}/V_{dc}	% Of Regulation $=\left[\frac{V_{NL}-V_L}{V_L}\right]\times 100$
1	100Ω						
2	500Ω						
3	1KΩ						
4	20KΩ						
5	40KΩ						
6	60KΩ						
7	80KΩ						
8	90KΩ						

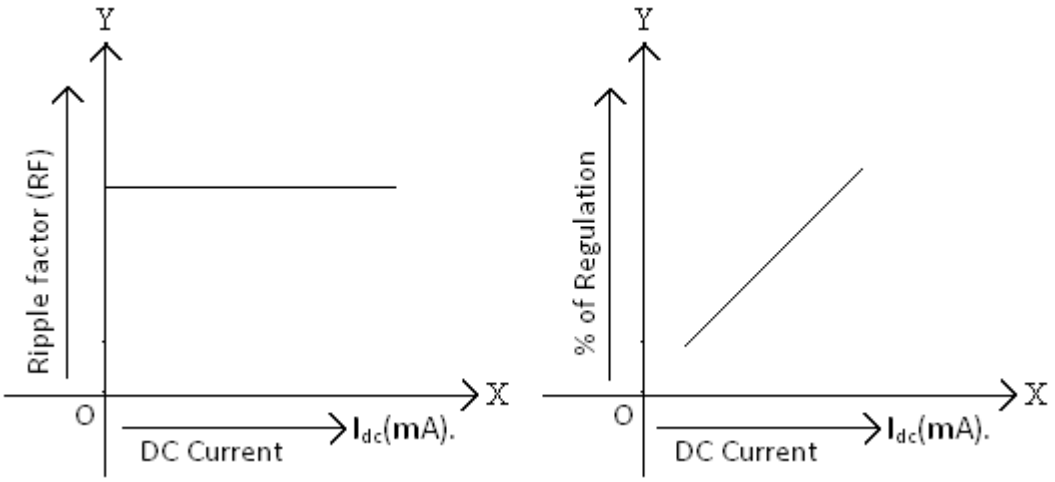
F). Full wave rectifier with 1000μF capacitor filter using Hardware :

No Load dc voltage (V_{NL}) =_____In volts.

Sl. No.	Load Resistance (R_L) In Ω/KΩ	DC current (I_{dc}) in mA.	DC Voltage (V_{dc} / V_L) in Volts.	AC voltage (V_{ac}) in Volts.	Theoretical Ripple Factor (R_F) = $\frac{1}{4\sqrt{3}(F \times C \times R_L)}$	Practical Ripple Factor (R_F)= V_{ac}/V_{dc}	% Of Regulation $=\left[\frac{V_{NL}-V_L}{V_L}\right]\times 100$
1	100Ω						
2	500Ω						
3	1KΩ						
4	20KΩ						
5	40KΩ						
6	60KΩ						
7	80KΩ						
8	90KΩ						

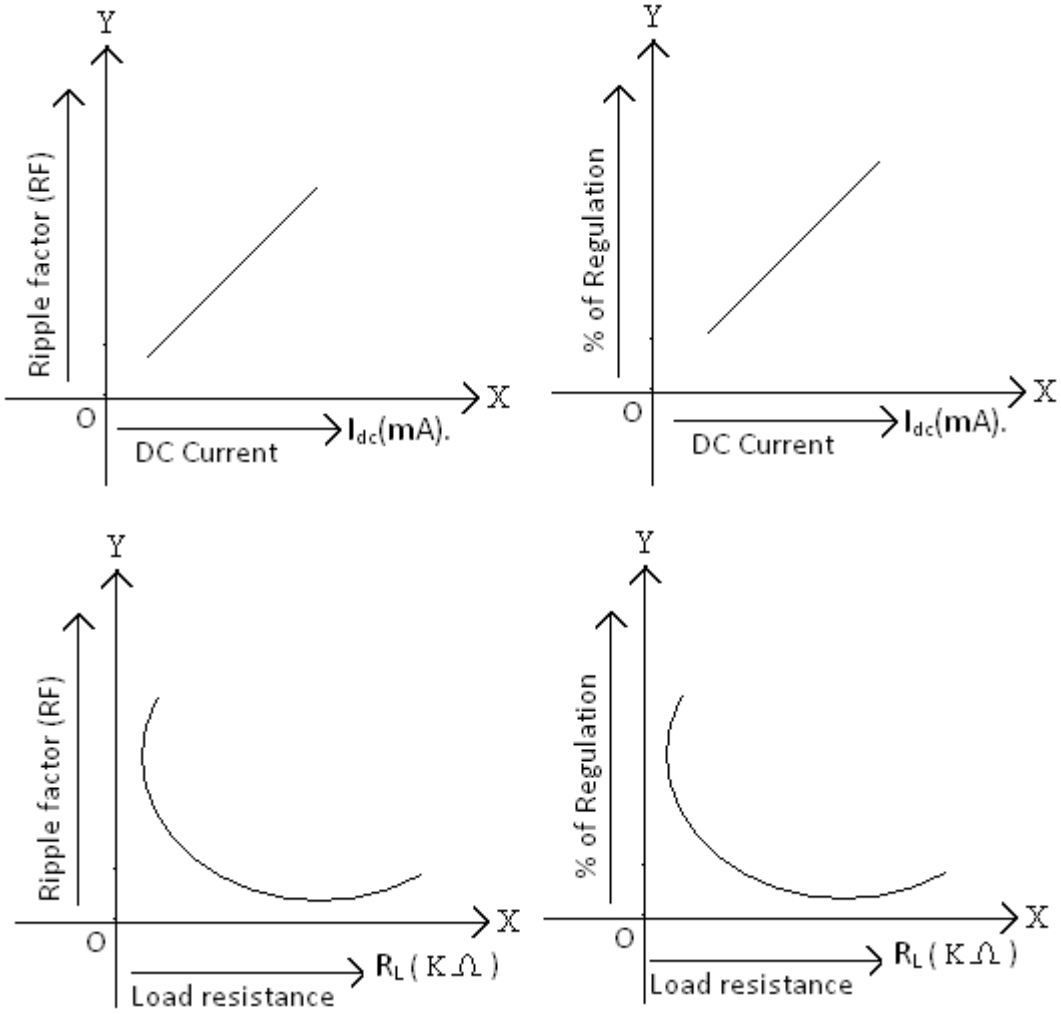
EXPECTED GRAPHS :

A). Full wave rectifier without filter :



B). Full wave rectifier With 100µF & 1000µF Filter (capacitor):

Note: Drawn the separate graph sheets for 100µF & 1000µF capacitors. i.e 4 graphs for 100µF and another 4 graphs for 1000µF capacitors as per given below,



EXPECTED WAVEFORMS:

A). Full wave rectifier without Filter :

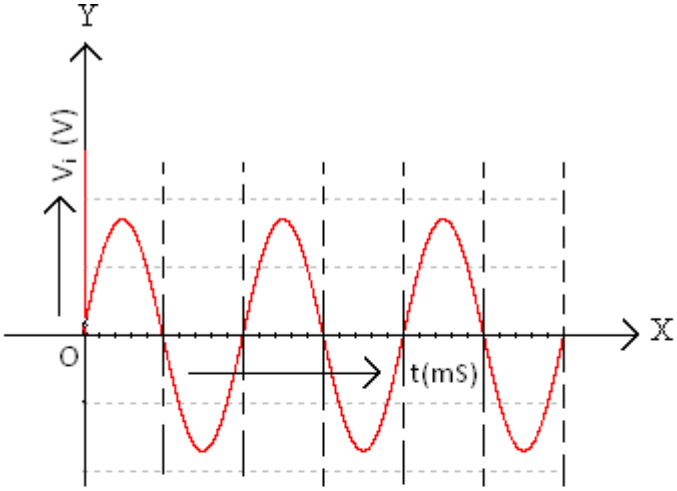


Figure: Input wave form for Full wave rectifier without filter

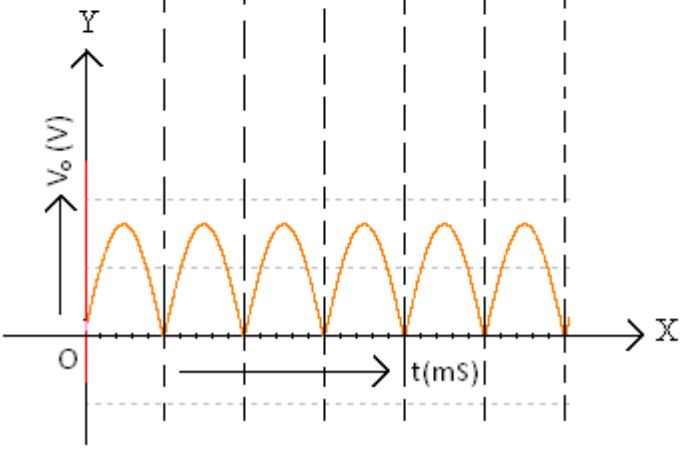


Figure: Output wave form for Full wave rectifier without filter , at R_L=1 KΩ

B). Full wave rectifier with 100µF Filter Filter (capacitor), at R_L=1KΩ:

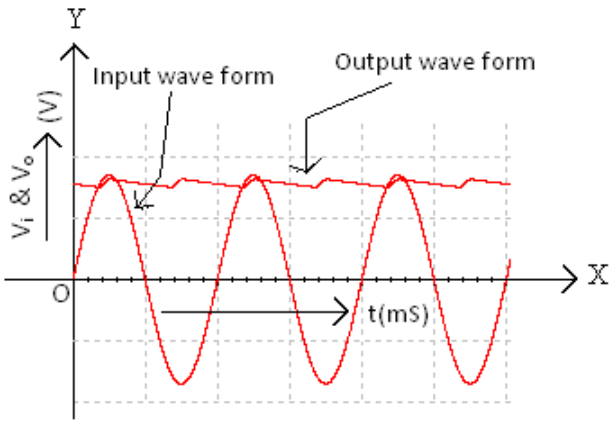


Figure: Input&Output waveforms for Full wave rectifier when 100 µF Filter (Capacitor) is connected at R_L=1 KΩ

C). Full wave rectifier with 1000µF (capacitor), at R_L=1KΩ:

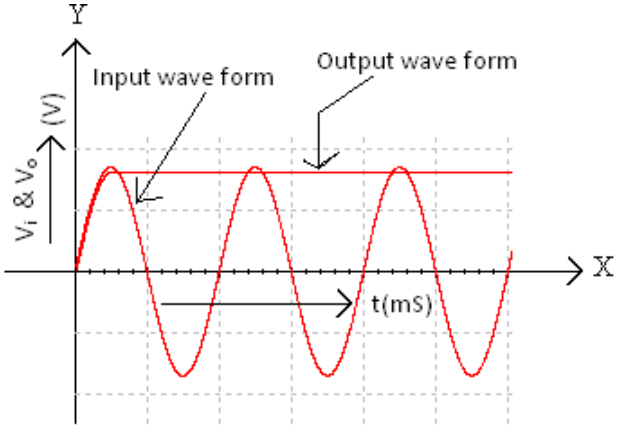


Figure: Input&Output waveforms for Full wave rectifier when 1000 µF Filter (Capacitor) is connected at R_L=1 KΩ

PARAMETERS OF FULL WAVE RECTIFEIR :

THEORETICAL VALUES	PRACTICAL VALUES
A). Without Filter: Ripple factor (RF) = 0.45	Ripple factor (RF) when R_L is at 1KΩ = *(Noted down from the tabular column).*
B). With 100µF capacitor: Ripple factor $RF = \frac{1}{4\sqrt{3}\,(F \times C \times R_L)} =$ Where, F = 50Hz., C=100µF, R_L=1KΩ	Ripple factor (RF) when R_L is at 1KΩ = *(Noted down from the tabular column).*
C). With 1000µF capacitor: Ripple factor $RF = \frac{1}{4\sqrt{3}\,(F \times C \times R_L)} =$ Where, F = 50Hz., C=1000µF, R_L=1KΩ	Ripple factor (RF) when R_L is at 1KΩ = *(Noted down from the tabular column).*

RESULT :

A). Without filter :

We studied the characteristics of *full wave rectifier without filter* and obtained the ripple factor , % of regulation at R_L=1KΩ. The values are given below,

1). Ripple factor(RF) =
2). 2). % of regulation =

B). With 100µF & 1000µF filter (capacitor) :

We studied the characteristics of *full wave rectifier with filter* and obtained the ripple factor , % of regulation at R_L=1KΩ. The values are given below,

1). Ripple factor(RF) for 100µF =
2). % of regulation for100µF =
3). Ripple factor(RF) for 1000µF =
4). % of regulation for 1000µF =

VIVA VOCE Questions :

1. What is Rectifier?

2. Classification of Rectifiers.

3. PIV for FWR is _____.

4. What is the Ripple Factor FWR?

5. What are the differences between Full Wave Center Tapped and Bridge Rectifier.

6. FWR consists of how many diodes?

7. What is the function of RPS?

8. What is the Efficiency of FWR?

9. What is the function of filter in Rectifiers?

10. Mention the properties of L and C components.

Exp. No. 3 Date :

CLIPPING AND CLAMPER CIRCUITS

AIM : To verify the various clipping and clamping circuits using PN junction diode in Hardware as well Using multisim software

APPARATUS :

1). Regulated power supply ------ 1No.
2). Function generator ------ 1 No.
3). Cahode Ray Oscilloscope (CRO) ------ 1 No.
4). System with Multisim software ------ 1 No.

COMPONENTS:

1). PN junction diode : 1N4007
2). Carbon fixed resistors 10 Ω , ½W, 10 KΩ , ½W ------ Each 1 No.

THEORY :

Most of the electronic circuits like amplifiers, modulators and many others have a particular range of voltages at which they have to accept the input signals. Any of the signals that have amplitude greater than this particular range may cause distortions in the output of the electronic circuits and may even lead to damage of the circuit components.

As most of the electronic devices work on a single positive supply, the input voltage range would also be on the positive side. Since the natural signals like audio signals, sinusoidal waveforms and many others contain both positive and negative cycles with varying amplitude in their duration.

These waveforms and other signals have to be modified in such a way that the single supply electronic circuits can be able to operate on them.

The clipping of a waveform is the most common technique that applies to the input signals to adapt them so that they may lie within the operating range of the electronic circuits. The clipping of waveforms can be done by eliminating the portions of the waveform which crosses the input range of the circuit.
Clippers can be broadly classified into two basic types of circuits. They are:

- Series Clippers
- Shunt or Parallel Clippers

Series clipper circuit contains a power diode in series with the load connected at the end of the circuit. The shunt clipper contains a diode in parallel with the resistive load.

CIRCUIT DIAGRAM :

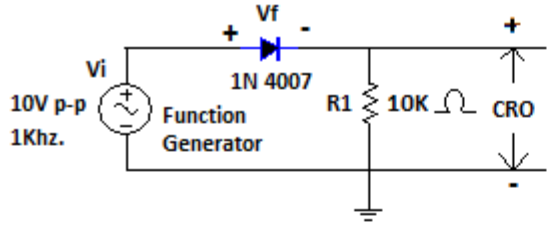


Fig (a) : Negative Series Clipper

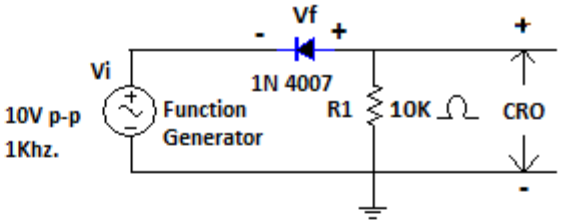


Fig (b) : Positive Series Clipper

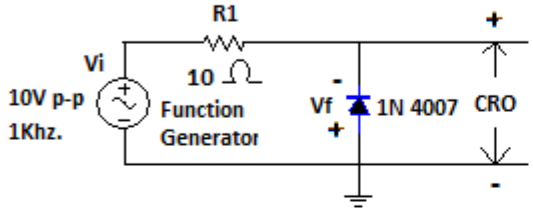


Fig (c) : Negative shunt Clipper

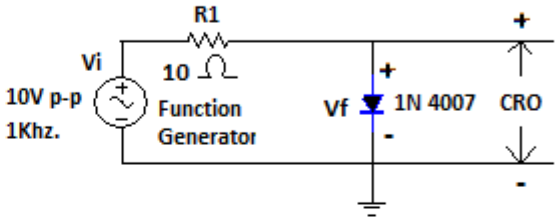


Fig (d) : Positive shunt Clipper

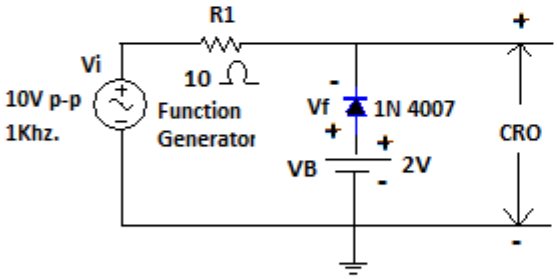


Fig (e) : Biased Clipper

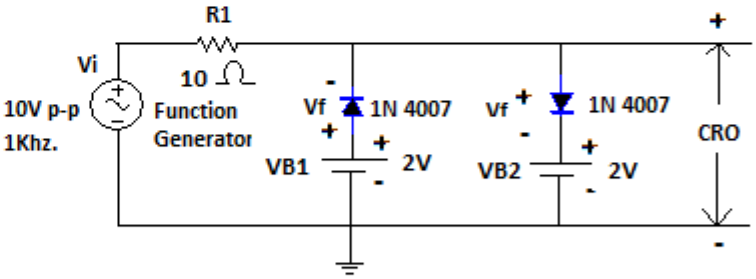


Fig (f) : Two level Clipper

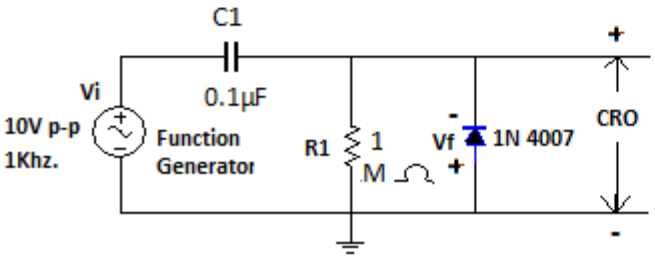


Fig (g) : Positive Clamper

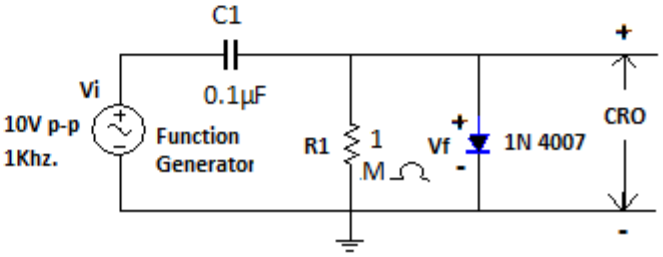


Fig (h) : Negative Clamper

PROCEDURE :

1). Connected the circuit as shown in the circuit diagram of figure (a)
2). Switched ON the Function generator and CRO.
3). Set the sine wave as $10V_{p-p}$ in the function generator.
4). Observed the wave forms in the CRO and draw in the graph sheets.
5). Repeated the same procedure for circuit diagrams of figures from b to h.
6). Repeated the same procedure using Multisim software.

EXPECTED WAVEFORMS :

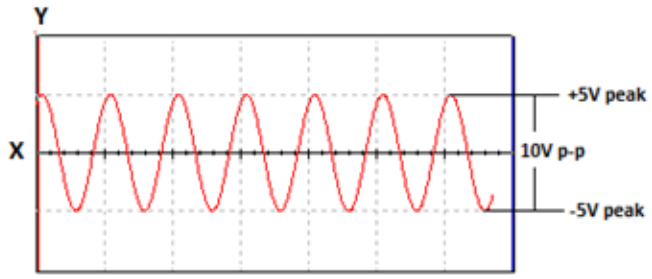


Fig (a) : Input wave form

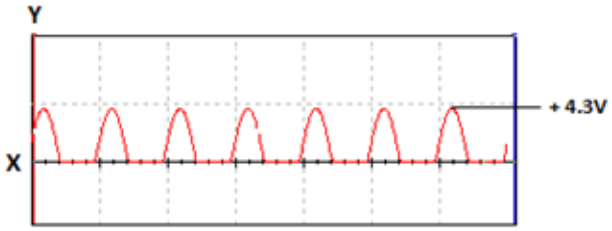


Fig (b) : Negative Series Clipper (CRO in DC mode)

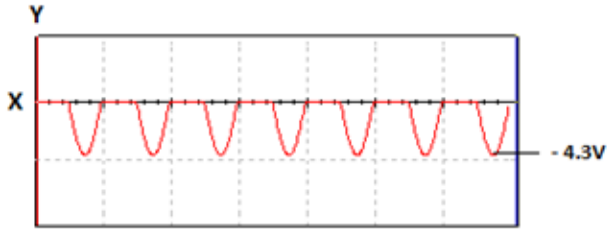


Fig (c) : Positive Series Clipper (CRO in DC mode)

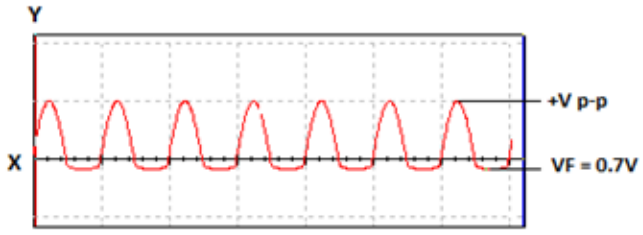


Fig (d) : Negative Shunt Clipper (CRO in DC mode)

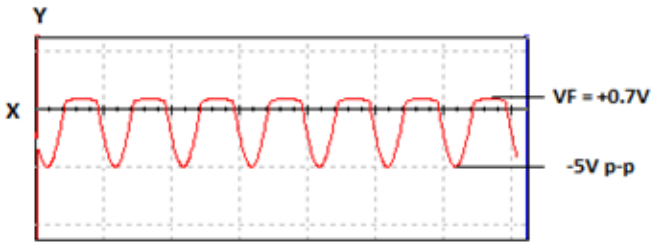


Fig (e) : Positive Shunt Clipper (CRO in DC mode)

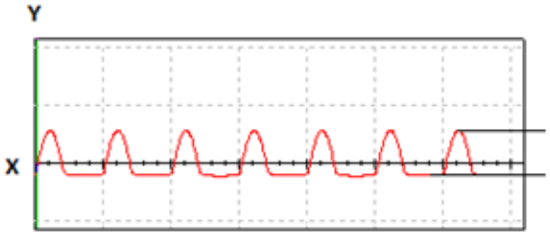


Fig (f) : Biased Clipper (CRO in AC mode)

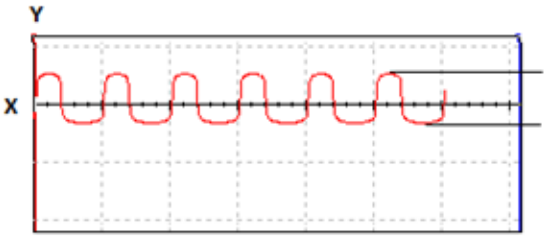


Fig (g) : Two level clipper (CRO in AC mode)

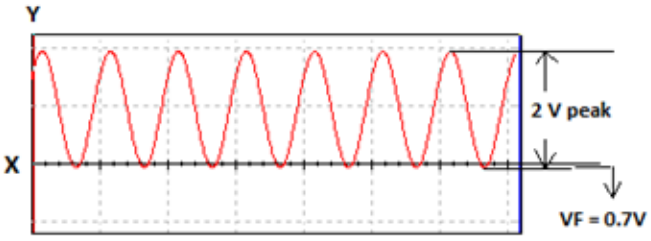


Fig (h) : Positive Clamper (CRO in DC mode)

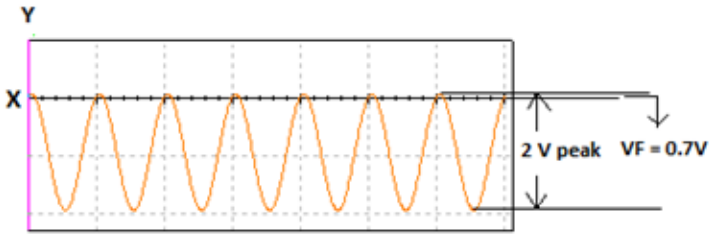


Fig (i) : Negative Clamper (CRO in DC mode)

For Figures b to e and h & i : Scale on X-axis : 1 Unit = 1mS
Y-axis : 1 Unit = 5V

For Figures f&g Scale on X-axis : 1 Unit = 1mS
Y-axis : 1 Unit = 2V

RESULT : We have observed and drawn the output and input wave forms of different types of Clippers and Clampers

VIVA VOCE Questions:

1. What is Clipper?

2. What is Clamper?

3. What is negative series clipper?

4. What is positive series clipper?

5. What is negative shunt clipper?

6. What is positive shunt clipper?

7. What is positive clamper?

8. What is negative clamper?

9. What is two- level clipper?

10. Importance of clippers and clampers.

Exp. No.		Date :
4	**ZENER DIODE**	

AIM :

1). To study the V-I characteristics of Zener diode
2). To obtain the regulation characteristics of a zener diode in the following conditions.
   a). By varying the input (supply) voltage,
   b). By varying the load resistance.
3). To design the Zener diode as voltage regulator.
4). All the above functions we could do in Hardware and multisim software.

APPARATUS :

1). Voltmeters	a). (0-10)V	Digital / Analog	DC Type	--- 1 No.
2). Ammeters	a). (0-50) mA	Digital / Analog	DC Type	--- 2 No.
3). Decade Resistance Box(DRB)				--- 1 No.
4). Regulated power supply (RPS)	(0-30)V, 1A	Dual channel		--- 1 No.
5). Bread board				--- 1 No.
6). Connecting wires				--- A few Nos.
7). System with Multisim software				--- 1 No.

COMPONENTS :

1). Zener diode 1Z6.9V, 1W	--- 1 No.
2). Carbon fixed resistors 150Ω	--- Each 1 No.

THEORY :

Explanation

A Zener Diode, also known as a breakdown diode, is a heavily doped semiconductor device that is designed to operate in the reverse direction. When the voltage across the terminals of a Zener diode is reversed and the potential reaches the Zener Voltage (knee voltage), the junction breaks down and the current flows in the reverse direction. This effect is known as the Zener Effect.

Definition

A Zener diode is a heavily doped semiconductor device that is designed to operate in the reverse direction. Zener diodes are manufactured with a great variety of Zener voltages (Vz) and some are even made variable.

How does a Zener Diode work in reverse bias?

A Zener diode operates just like a normal diode when it is forward-biased. However, when connected in reverse biased mode, a small leakage current flows through the diode. As the reverse voltage increases to the predetermined breakdown voltage (Vz), current starts flowing through the diode. The current increases to a maximum, which is determined by the series resistor, after which it stabilizes and remains constant over a wide range of applied voltage.

There are two types of breakdowns for a Zener Diode:

- **Avalanche Breakdown**
- **Zener breakdown**

Avalanche Breakdown in Zener Diode

Avalanche breakdown occurs both in normal diode and Zener Diode at high reverse voltage. When a high value of reverse voltage is applied to the PN junction, the free electrons gain sufficient energy and accelerate at high velocities. These free electrons moving at high velocity collides other atoms and knocks off more electrons.

Due to this continuous collision, a large number of free electrons are generated as a result of electric current in the diode rapidly increases

This sudden increase in electric current may permanently destroy the normal diode, however, a Zener diode is designed to operate under avalanche breakdown and can sustain the sudden spike of current. Avalanche breakdown occurs in Zener diodes with Zener voltage (Vz) greater than 6V.

Zener Breakdown in Zener Diode

When the applied reverse bias voltage reaches closer to the Zener voltage, the electric field in the depletion region gets strong enough to pull electrons from their valence band. The valence electrons that gain sufficient energy from the strong electric field of the depletion region break free from the parent atom. At the Zener breakdown region, a small increase in the voltage results in the rapid increase of the electric current.

Design : Design a voltage regulator circuit using Zener diode for the following conditions ,

$V_O = 6.9V$, $V_{in} = (10\text{-}20)$, $I_L = (20\text{-}45)$ mA , $I_Z = (10\text{-}30)$mA

Sol :

a). Finding the power rating of Zener diode

$V_Z = V_O = 6.9V$ $I_{Z(max)} = 30mA$

$P_Z = V_Z \times I_{Z(max)} = 6.9V \times 30 \times 10^{-3} = 0.20W$

Hence Choose 6.9V, 0.25W Zener diode

b). Finding the Load Resistance R_L and its its Power rating P_{RL}

$$R_{L(min)} = \frac{V_O}{I_{L(max)}} = \frac{6.9V}{45 \times 10^{-3}} = 153.33\,\Omega \Rightarrow 150\,\Omega$$

$$R_{L(max)} = \frac{V_O}{I_{L(min)}} = \frac{6.9V}{20 \times 10^{-3}} = 345\,\Omega \Rightarrow 330\,\Omega$$

Power through Load Resistor at $R_{L(min)}$

$P_{RL} = (I_{L(max)})^2 \times R_{L(min)} = (45 \times 10^{-3})^2 \times 150\,\Omega$

$P_{RL} = 0.30$Watt

0.30W resistor not avail in the market, So we can choose 0.5 Watt resistor.

c). Finding the value of Input Resistance, R and its Power rating P_R

$$R_{max} = \frac{V_{in(max)} - V_O}{I_{L(min)} + I_{Z(max)}} = \frac{20 - 6.9V}{(20 + 30) \times 10^{-3}} = 262\,\Omega$$

$$R_{min} = \frac{V_{in(min)} - V_O}{I_{L(max)} + I_{Z(min)}}$$

$$R_{min} = \frac{10 - 6.9V}{(45 + 10) \times 10^{-3}} = 56.36\,\Omega$$

$$R = \frac{R_{max} + R_{min}}{2}$$

$$R = \frac{262\,\Omega + 56.36\,\Omega}{2} = 159\,\Omega \Rightarrow 150\,\Omega$$

Current through Series Resistor, $I = I_{Z(max)} + I_{L(max)}$

$I = 30mA + 45mA = 75mA$

Power through Series Resistor $P_R = I^2 \times R_{max}$

$P_R = (75 \times 10^{-3})^2 \times 262\,\Omega = 1.47$ Watt

1.47W Resistor not avail in the market, So we can choose 2Watt Resistor.

CIRCUIT DIAGRAM :

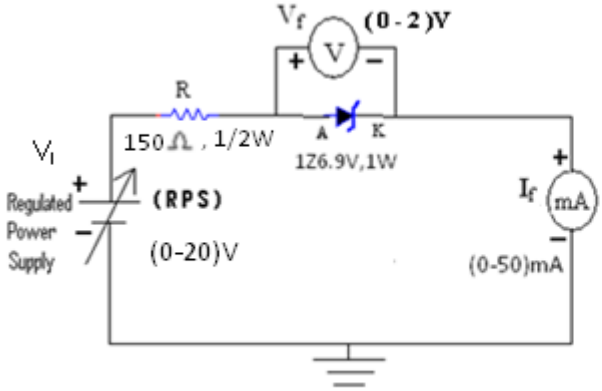


Fig (a) : Zener diode in forward bias

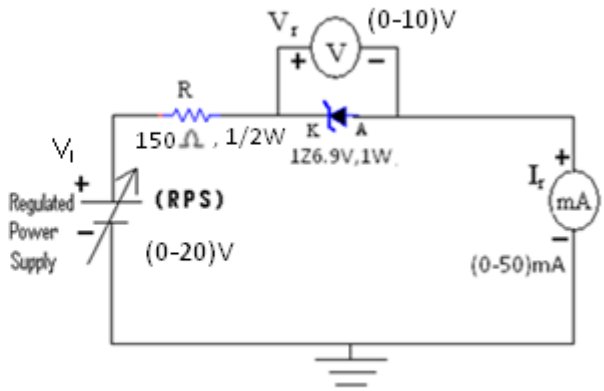


Fig (b) : zener diode in Reverse bias

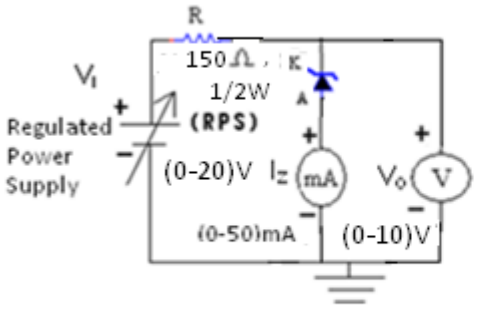


Figure (c): Zener diode as voltage Regulator by varying input voltage

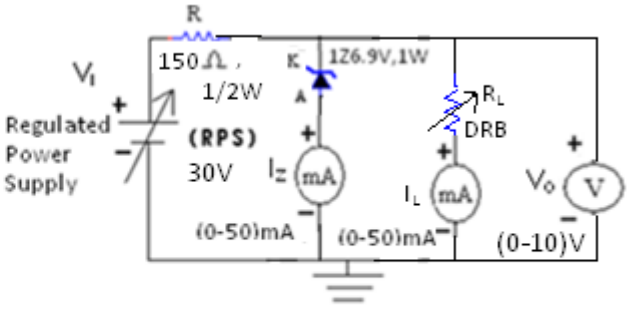


Figure (d) : Zener diode as Voltage regulator by varying Load resistance

PROCEDURE :

A). VI characteristics of Zener diode in Forward bias :

1). Connected the circuit for diode *1Z6.9V* as shown in the circuit diagrams (a).
2). Connected the positive terminal of the RPS to the Anode(A), negative terminal of the RPS to the Cathode(C) of the Zener diode respectively.
3). Then Switched ON the RPS and all the meters.
4). Varied the supply voltage (RPS voltage) in steps i.e. 0V, 1V, 5V, 10V, 15V, 20V and noted down the corresponding readings of voltmeter V_f (In volts) and millimeter I_f (In mA) of tabular column (A).
5). After completion of readings kept the RPS voltage at 0V immediately.
6). Then Switched OFF the RPS and all the meters.
7). Plotted the graph between *reverse voltage(V_f)* on X-axis and *reverse current (I_f)* on Y-axis in graph sheet using the values in tabular column (A).
8). Calculated the *static resistance* and *dynamic resistance* from the graph sheet by using the formulas which are given under the heading of parameters.
9). Repeated the same procedure in Multisim software also, noted down the readings under the tabular column of multisim.

B). VI characteristics of Zener diode in Reverse bias :

1). Connected the circuit as shown in the diagrams (b).
2). Connected the positive terminal of the RPS to the Cathode(C). negative terminal of the RPS to the Anode(A) of Zener diode respectively.
3). Then Switched ON the RPS and all the meters.
4). Varied the supply voltage (RPS voltage) in steps i.e. 0V, 1V, 5V, 10V, 15V, 20V and noted down the corresponding readings of voltmeter V_r (In volts) and millimeter I_r (In mA) in tabular column (B).
5). After completion of readings kept the RPS voltage at 0V immediately.
6). Then Switched OFF the RPS and all the meters.
7). Plotted the graph between *reverse voltage(V_r)* on X-axis and *reverse current (I_r)* on Yaxis in the graph sheet using the values in tabular column (B).
8). Calculated the *static resistance* and *dynamic resistance* from each graph sheet by using the formulas which are given under the heading of parameters.
9). Repeated the same procedure in Multisim software also, noted down the readings under the tabular column of multisim.

C). As voltage regulator by varying the Input (supply) voltage at no R_L :

1). Connected the circuit for diode *1Z6.9V* as shown in the circuit diagrams (c).
2). Then Switched ON the RPS and all the meters.
4). Varied the input voltage V_i (RPS voltage) in steps i.e. 0V, 1V, 5V, 10V, 15V, 20V and noted down the corresponding readings in tabular column (C).
5). Up to the break down point the output voltage V_O will increase linearly with respect to variation in the input voltage, after the break down voltage the output voltage V_O is constant.
6). After completion of readings kept the RPS voltage at 0V immediately.
7). Then Switched OFF the RPS and all the meters.
8). Plotted the graph between *input voltage (V_i)* on X-axis and *output voltage (V_O)* on Y- axis in the graph sheet using the values in tabular column (C).
9). Repeated the same procedure in Multisim software also, noted down the readings under the tabular column of multisim.

D). As voltage regulator by varying the Input (supply) voltage at R_L = 330Ω &150Ω :

1). Connected the circuit for diode *1Z6.9V* as shown in the circuit diagram (d).
2). Then Switched ON the RPS and all the meters.
3). Keep $R_{L(max)}$ in DRB as 330Ω.
4). Varied the input voltage V_i (RPS voltage) in steps i.e. 0V, 1V, 5V, 10V, 15V, 20V and noted down the corresponding readings in tabular column (D).
5). Up to the break down point the output voltage V_O will increase linearly with respect to variation in the input voltage, after the break down voltage the output voltage V_O is constant.
6). After completion of readings keep the RPS voltage at 0V immediately.
7). Kept $R_{L(min)}$ in DRB as 150Ω
8). Repeated the same procedure from step 4 to 6 but noted down the readings in tabular column (E).
9). Then Switched OFF the RPS and all the meters.
10). Plotted the graph between *input voltage (V_i)* on X-axis and *output voltage*

(V_O) on Y- axis in the graph sheet using the values in tabular column (E).

11). Repeated the same procedure in Multisim software also, noted down the readings under the tabular column of multisim.

E). As voltage regulator by varying the load resistance (R_L) at V_i = 20V & 10V:

1). Connected the circuit for diode *1Z6.9V* as shown in the circuit diagram (d).
2). Then Switched ON the RPS and all the meters.
3). Kept the RPS voltage at constant value 20V up to the completion of readings.
4). Noted down the readings of Zener current (I_z), Load current (I_L) and Output voltage(V_O) by varying the load resistance in steps 47Ω, 150Ω, 220Ω), 330Ω, 560Ω in tabular column (F).
5). After completion of readings kept the RPS voltage at 0V immediately.
6). Now this time kept the RPS voltage as constant as 10V.
7). Repeated the same procedure from steps 4 to 5. But these corresponding readings are noted down in the tabular column (G).
8). Then switched OFF the RPS and all the meters.
9). Plotted the graph between *output voltage (V_O)* on X-axis and *load current (I_L)* on Yaxis in graph sheet using the values in tabular column (F).
10). Repeated the same procedure in Multisim software also, noted down the readings under the tabular column of multisim.

TABULAR COLOUMNS :

A). Zener diode in Forward bias : **B). Zener diode in Reverse bias :**

Using Hardware : Using Multisim software Using Hardware :Using Multisim software :

Sl. No	V_i (V)	V_f (V)	I_f (mA)		Sl. No	V_f (V)	I_f mA)		Sl. No	V_i (V)	V_r (V)	I_r (mA)		Sl. No	V_i (V)	V_r (V)	I_r (mA)
1	0				1	0			1	0				1	0		
2	5				2	5			2	5				2	5		
3	10				3	10			3	10				3	10		
4	15				4	15			4	15				4	15		
5	20				5	20			5	20				5	20		

C). Zener diode as Voltate Regulator as Input voltage varies at no R_L :

Using Hardware : Using Multisim software :

Sl. No.	V_i (V)	V_O (V)	I_Z (mA)		Sl.No.	V_i (V)	V_O (V)	I_Z (mA)
1	0				1	0		
2	5				2	5		
3	10				3	10		
4	15				4	15		
5	20				5	20		

D). When V_i varies at $R_{L(max)}$ = 330Ω,

Using Hardware *:* Using Multisim software :

Sl.No.	V_i (V)	I (mA)	I_Z (mA)	I_L (mA)	V_O or V_Z (V)		Sl.No.	V_i (V)	I (mA)	I_Z (mA)	I_L (mA)	V_O or V_Z (V)
1	0						1	0				
2	5						2	5				
3	10						3	10				
4	15						4	15				
5	20						5	20				

E). When V_i varies at $R_{L(min)}$ = 150Ω,

Using Hardware *:* Using Multisim software :

Sl.No.	V_i (V)	I (mA)	I_Z (mA)	I_L (mA)	V_O or V_Z (V)		Sl.No.	V_i (V)	I (mA)	I_Z (mA)	I_L (mA)	V_O or V_Z (V)
1	0						1	0				
2	5						2	5				
3	10						3	10				
4	15						4	15				
5	20						5	20				

F). When R_L varies at V_i = 20V

Using Hardware *:* Using Multisim software :

Sl.No.	R_L (Ω)	I (mA)	I_Z (mA)	I_L (mA)	V_O or V_Z (V)		Sl.No.	V_i (V)	I (mA)	I_Z (mA)	I_L (mA)	V_O or V_Z (V)
1	47						1	5				
2	150						2	10				
3	220						3	15				
4	330						4	20				
5	560						5	30				

G). When R_L varies at V_i = 10V

Using Hardware *:* Using Multisim software :

Sl.No.	R_L (Ω)	I (mA)	I_Z (mA)	I_L (mA)	V_O or V_Z (V)		Sl.No.	V_i (V)	I (mA)	I_Z (mA)	I_L (mA)	V_O or V_Z (V)
1	47						1	5				
2	150						2	10				
3	220						3	15				
4	330						4	20				
5	560						5	30				

EXPECTED GRAPHS :

A). Reverse bias characteristics of Zener diode

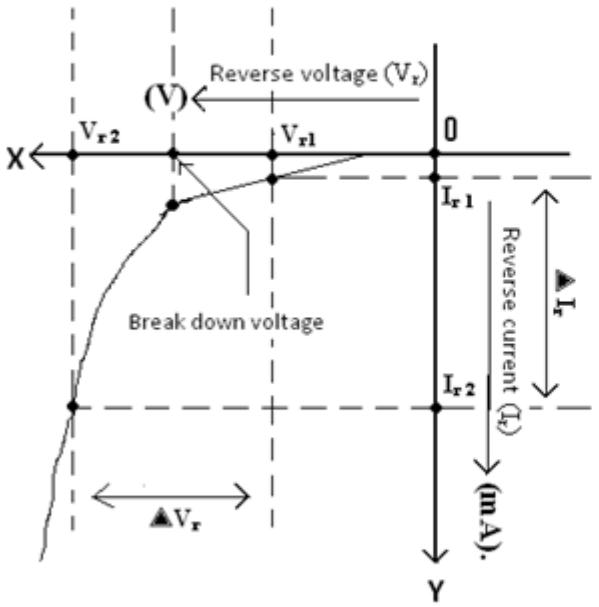


Figure: Reverse bias characteristics of Zener diode using 1Z6.9V

B). Regulation characteristics of Zener diode by varying supply voltage.

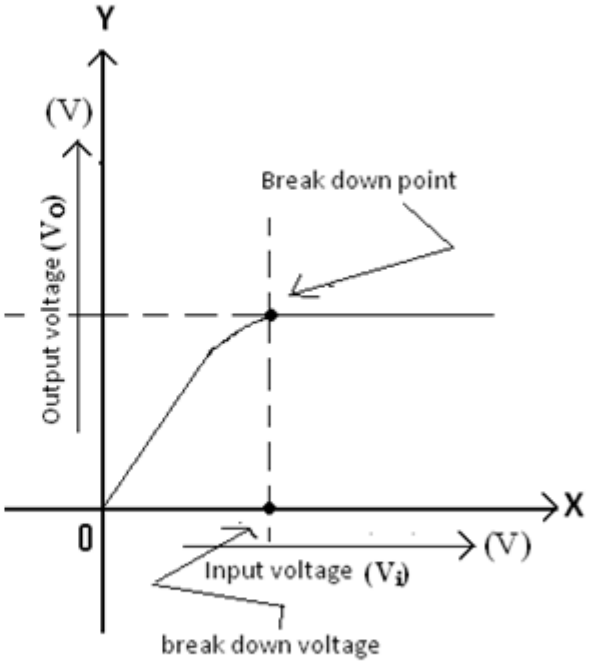


Figure: Regulation characteristics of zener diode by varying supply voltage using 1Z6.9V

C). Regulation characteristics of Zener diode by varying load resistance :

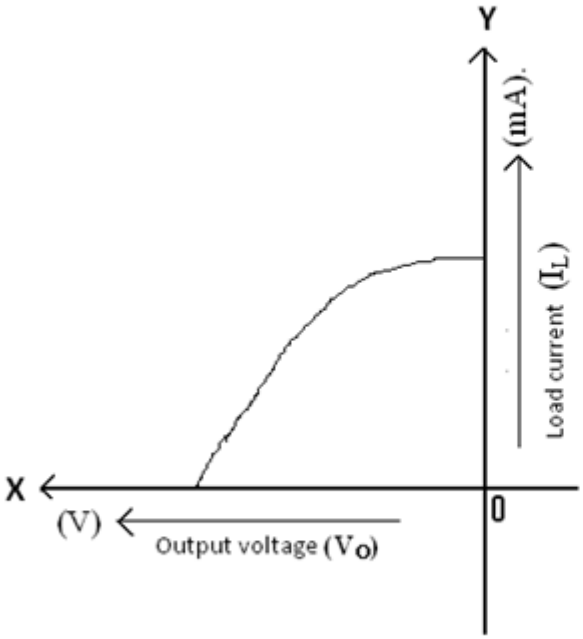


Figure: Regulation characteristics of Zener diode by varying load resistance using 1Z6.9V

PARAMETERS :

A). V-I Characteristics of Reverse bias using 1Z6.9V

1). Static resistance : V_r / I_r =

2). Dynamic resistance : $\blacktriangle V_r / I_r$ =

RESULT :

We design and studied the V-I & Regulation characteristics of Zener diode in Forward bias and Reverse bias .

1). Static resistance :

2). Dynamic resistance :

VIVA VOCE Questions:

1. What is zener diode?

2. What is Regulator?

3. Difference between Zener diode and PN diode?

4. What is zener break down?

5. What is static resistance?

6. What is dynamic resistance?

7. Applications of zener diode?

8. What is the principle mechanism of zener diode?

9. What is Regulation?

10. Any Draw backs in zener diode?

Exp. No. Date :

5 JFET CHARACTERISTICS - COMMON SOURCE CONFIGURATION

AIM :

1). To study the static and transfer characteristics of the FET using Hardware and multisim software
2). To calculate the following FET parameters
(a). Drain resistance (r_d) (b). Trans conductance (gm) (c). Amplification factor (μ)
(d) Pinch-off voltage(V_P).

APPARATUS :

1). Voltmeters :	(0-2)V	Digital	DC Type	----- 1 No.
	(0-50)V	Digital/Analog	DC Type	----- 1 No.
2). Ammeters :	(0-20)mA	Digital/Analog	DC Type	----- 1 No.
3). Regulated Power Supply (RPS) : 30V, 1A		Dual channel		----- 1 No.
4). Bread board :				----- 1 No.
5). Connecting wires :				----- A few Nos.
6). System with multisim software				----- 1 No.

COMPONENTS :

1). Field Effect Transistor (FET) :	BF W11	----- 1 No.
2). Carbon fixed resistors	22Ω, ½W and 1K KΩ ,½W	----- Each 1 No.

THEORY :

The Field Effect Transistor or Simply FET uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage, the Gates to source junction of the FET is always reversed biased. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the Field Effect Transistor a "VOLTAGE" operated device.

The Field Effect Transistor is a three terminal unipolar semiconductor device that has very similar characteristics to those of their Bipolar Transistor counterpart's i.e., high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT).

The Field Effect Transistor has one major advantage over its standard bipolar transistor, in that input impedance, (Rin) is very high, (thousands of Ohms). This very high input impedance makes them very sensitive to input voltage signals.

There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET is always reverse biased.

In amplifier application, the FET is always used in the region beyond the pinch-off.

CIRCUIT DIAGRAM :

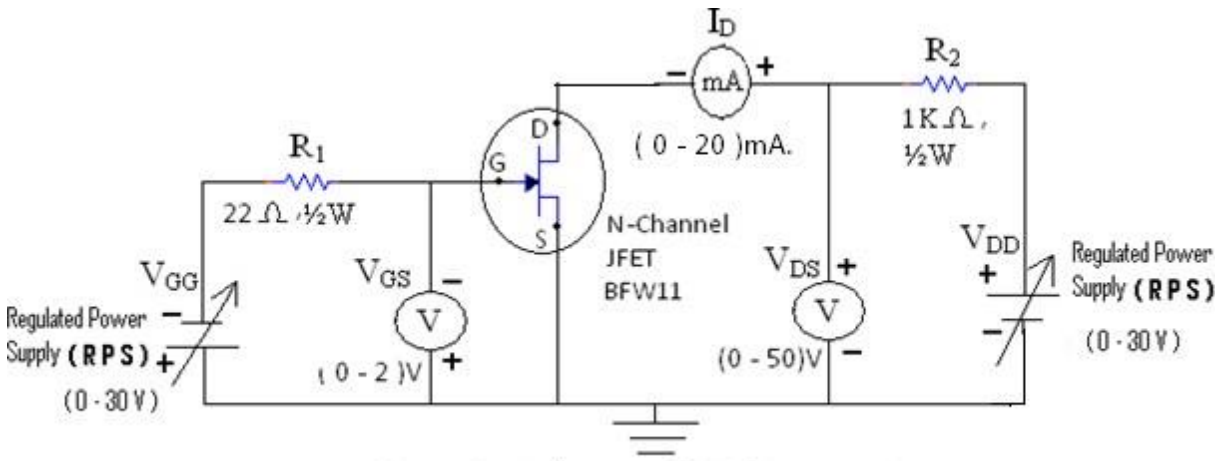


Figure: Circuit diagram of FET characteristics

PROCEDURE :

A). Transfer characteristics :

1). Connected the circuit as per the circuit diagram.
2). Switched ON the RPS and all the meters.
3). Kept the V_{DS} voltage at constant 2V by varying the drain forward voltage i.e. $V_{DD.}$
4). Varied the gate reverse voltage V_{GG} in steps of 0.00V, 0.40V, 0.80V, 1.2V, 1.6V, 2.0V and noted down the corresponding readings of V_{GS} and I_D meters.
5). Now kept the V_{GG} is at 0V.
6). Repeated the same procedure from step 4 to step 5 for V_{DS}=4V by varied the V_{DD}.
7). Switched OFF the RPS and all the meters.
8). Plotted the graph between V_{GS} on X-axis and I_D on Y-axis.
9). Calculated the *transconductance* value from the graph as per the formula which is given under the heading of *parameters.*

Note: *Do not vary the supply voltage V_{DD} unless V_{GG} is kept at 0 Volts.*

10). We did the same experiment in multisim software also and noted down the corresponding readings in the tabular column (A).

B). Static/Drain characteristics :

1). Connected the circuit as shown in the circuit diagram.
2). Now Switched *ON* the *RPS* and all the meters.
3). Kept the V_{GS} = 0V by varying the supply voltage $V_{GG.}$
4). Varied the supply voltage V_{DD} in steps of 0.0V, 0.50V, 1.0V, 2.0V, 4.0V, 6.0V,8.0V, 10.0V, 12.0V, 14.0V, 16.0V, 18.0V, 20.0V, 24.0V, 28.0V, 30.0V and noted down the corresponding readings of V_{DS} and I_D meters.
5). Now kept the V_{DD} is at 0V.
6). Repeated the same procedure from steps 4 to 5 for each time independently when V_{GS} = -0.5V&V_{GS} = - 01.00V by varying the V_{GG}.
7). Now switched OFF the RPS and all the meters.

Note: *Do not vary the supply voltage V_{GG} unless V_{DD} is kept at 0 Volts.*

8). Plotted the graph between V_{DS} on X-axis and I_D on Y-axis.
9). Calculated the *drain resistance* value from the graph and *amplification factor* as per the formulas which are given under the heading of *parameters.*

10). We did the same experiment in multisim software also and noted down the corresponding readings in the tabular column (B).

TABULAR COLUMNS :

A). Transfer Characteristics :

Using Hardware : Using Multisim software :

SL. No.	V_{GG} (V)	V_{DS} = 2V		V_{DS} = 4V			V_{DS} = 2V		V_{DS} = 4V	
		V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)		V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)
01	00.00									
02	00.40									
03	00.80									
04	01.20									
05	01.60									
06	02.00									

B). Static / Drain Characteristics :

Using Hardware : Using Multisim software :

SL. No.	V_{DD} (V)	V_{GS} = 0V		V_{GS} = 0.5V		V_{GS} = 1V			V_{GS} = 0V		V_{GS} = 0.5V		V_{GS} = 1V	
		V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)		V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)
01	00.00													
02	00.50													
03	01.00													
04	02.00													
05	04.00													
06	06.00													
07	08.00													
08	10.00													
09	12.00													
10	14.00													
11	16.00													
12	18.00													
13	20.00													
14	24.00													
15	28.00													
16	30.00													

EXPECTED GRAPHS :

A). Transfer characteristics :

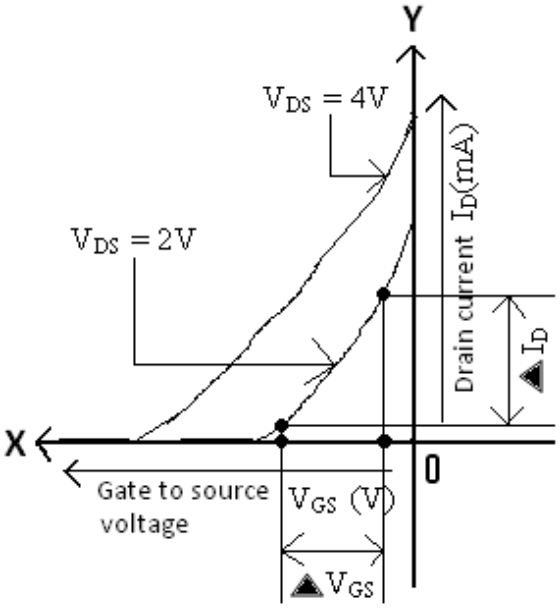


Figure: Measurement of h- parameters of FET in transfer characteristics.

B). Static/drain characteristics :

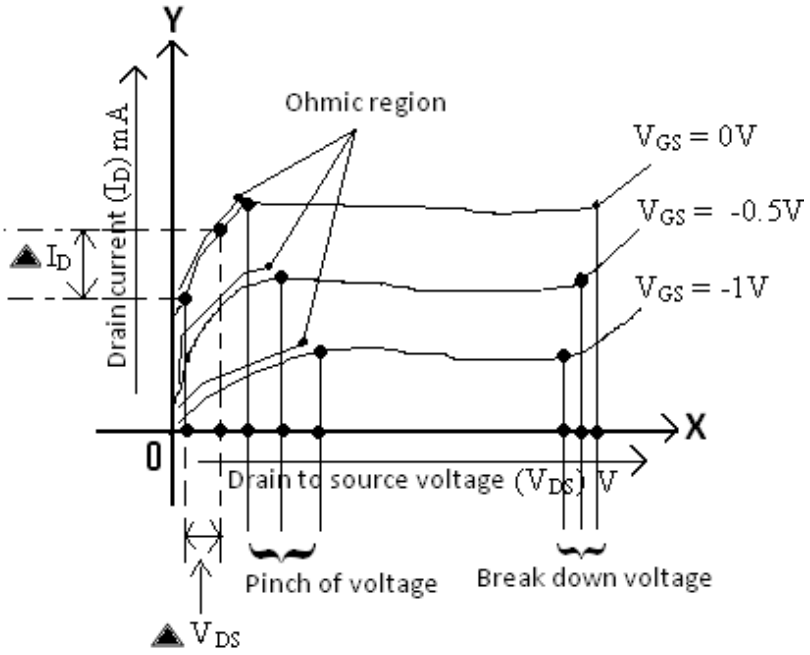


Figure: Measurement of h- parameters of FET in static/drain characteristics.

PARAMETERS :

1). Transconductance $(g_m) = \Delta I_D / \Delta V_{GS}$ At V_{DS} is constant.

=

(Calculated from transfer characteristics curve)

2). Drain resistance $(r_d) = \Delta V_{DS} / \Delta I_D$ At V_{GS} is constant.

=

(Calculated from static/drain characteristics curve)

3). Amplification factor (g_m) = Drain resistance (r_d) × Transconductance (g_m).

=

4). Pinch off Voltage (V_P) =

RESULT :

The *transfer* and *static/drain* characteristics are observed. The parameters *drain resistance (r_d), trans conductance (g_m)* and *amplification factor (μ)* are calculated.

VIVA VOCE QUESTIONS:

1. What is the Difference between BJT and FET?

2. What are the transfer characteristics?

3. What are the drain characteristics?

4. What are the applications of FET?

5. FET is which controlled device?

6. Mention FET characteristics.

7. What are the configurations of FET?

8. What are the classifications of FET?

9. Which configuration mostly used in FET?

10. What are the advantages of FET?

Exp. No. Date :

6 BJT CHARACTRISTICS - COMMON EMITTER (CE) CONFIGURATION

AIM : **To obtain the input and output characteristics of transistor in *Common Emitter Configuration*** using Hard ware and multisim software

APPARATUS :

1). Voltmeters :	(0 – 2)V	Digital	DC Type	------- 1 No.
	(0 – 50)V	Digital / Analog	DC Type	------- 1 No.
2). Ammeters :	(0 – 20)mA	Digital / Analog	DC Type	------- 1 No.
	(0 – 2000)µA	Digital only	DC Type	------- 1 No.
3). Regulated Power Supply (RPS) :	(0-30)V, 1A	Dual channel		-------- 1 No.
5). Bread board :				-------- 1 No.
5). Connecting wires :				-------- A few Nos.
6). System with multisim :				

COMPONENTS :

1). Transistor :	BC 547	-------- 1 No.
2) Carbon fixed resistors	a). 1 KΩ ,½W	-------- 1 No.
	b). 33 KΩ, ½W	-------- 1 No.

THEORY :

The transistor is a two junction, three terminal semiconductor device which has three regions namely the emitter region, the base region, and the collector region. There are two types of transistors. An npn transistor has an n type emitter, a p type base and an n type collector while a pnp transistor has a p type emitter, an n type base and a p type collector. The emitter is heavily doped, base region is thin and lightly doped and collector is moderately doped and is the largest. The current conduction in transistors takes place due to both charge carriers- that is electrons and holes and hence they are named Bipolar Junction Transistors (BJT).

BJTs are used to amplify current, using a small base current to control a large current between the collector and the emitter. This amplification is so important that one of the most noted parameters of gain, β (or hFE), which is the ratio of collector current to base current. When the BJT is used with the base and emitter terminals as the input and the collector and emitter terminals as the output, the current gain as well as the voltage gain is large. It is for this reason that this common-emitter (CE) configuration is the most useful connection for the BJT in electronic systems

Operation regions and characteristics curves: Depending upon the biasing of the two junctions, emitter-base (EB) junction and collectorbase(CB) the transistor is said to be in one of the four modes of operation. as described below:

Operating region	**B-E Junction**	**B-C Junction**	**Features**			
Cut-off	Reverse	Reverse	IB ≈ IC≈IE≈0	Off state – no current (VBE<0.7V)		
Saturation	Forward	Forward	Conducting structure	VBE=0.7V	VCE ≈ 0.2V	
Active	Forward	Reverse	Amplifier Gain: 100-1000	(IC=βIB)	VBE=0.7V	VCE >0.2V
Reverseactive	Reverse	Forward	Limited use Gain< 1	(IB >IC)		

NOTE : VBE will vary from 0.6 to 0.7 V

The most important characteristics of transistor in any configuration are input and output characteristics. A. Input Characteristics: - It is the curve between input current IB and input voltage VBE constant collector emitter voltage VCE. The input characteristic resembles a forward biased diode curve. After cut in voltage the IB increases rapidly with small increase in VBE. It means that dynamic input resistance is small in CE configuration. It is the ratio of change in VBE to the resulting change in base current at constant collector emitter voltage. It is given by ΔVBE / ΔIB B. Output Characteristics: - This characteristic shows relation between collector current IC and collector voltage for various values of base current. The change in collector emitter voltage causes small change in the collector current for the constant base current, which defines the dynamic resistance and is given as ΔVCE / ΔIC at constant IB. The output characteristic of common emitter configuration consists of three regions: Active, Saturation and Cut-off

Active region: In this region base-emitter junction is forward biased and base-collector junction is reversed biased. The curves are approximately horizontal in this region.

Saturation region: In this region both the junctions are forward biased.

Cut-off : In this region, both the junctions are reverse biased. When the base current is made equal to zero, the collector current is reverse leakage current ICEO. The region below IB = 0 is the called the cutoff region.

CIRCUIT DIAGRAM :

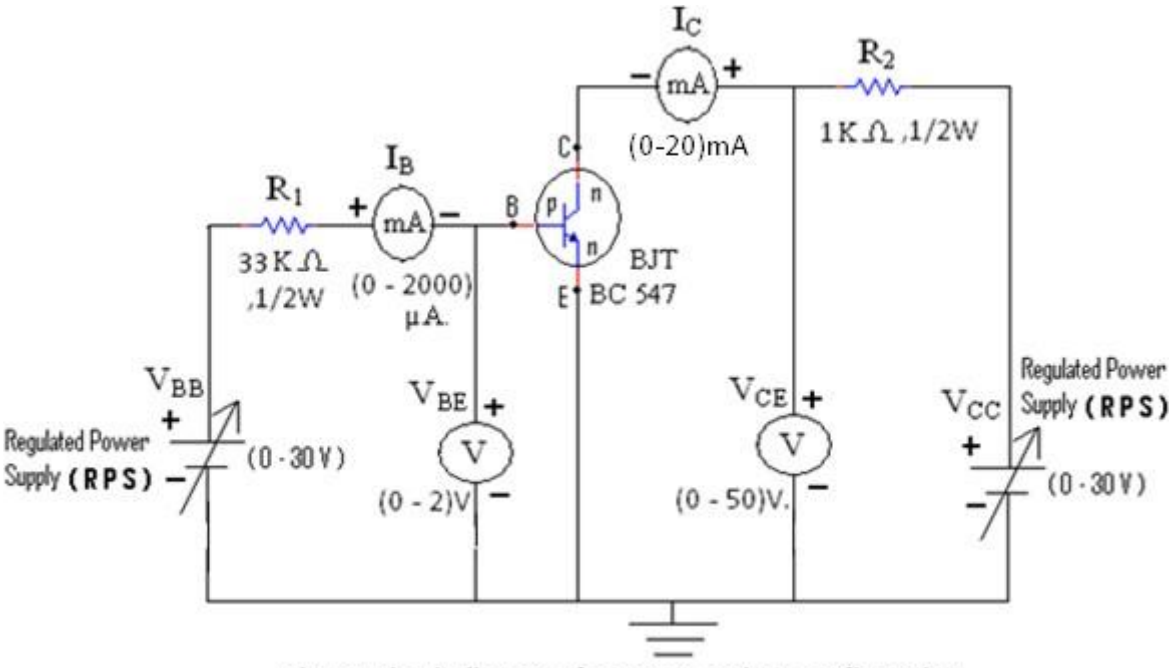


Figure: Circuit diagram of Common emitter configuration.

PROCEDURE :

A). Input characteristics :

1). Connected the circuit as shown in the circuit diagram.
2). Now Switched *ON* the *RPS* and all the meters.
3). Kept the V_{CE} = 0V by adjusted the V_{CC}.
4). Varied the supply voltage V_{BB} in steps of 0.0V, 0.50V, 1V, 2V, 4V, 6V, 8V, 10V, 15V,20V, 25V, 30V and noted down the corresponding readings of V_{BE} and I_B the meters.
5). Kept the V_{BB} at 0V.
6). Repeated the same procedure from steps 4 to 5 for each time independently when V_{CE} = 1V & V_{CE} = 2V which are kept by varying the V_{CC}.
7). Now switched OFF the RPS and all the meters.
8). 8). Took care that
   a). The values of V_{BE} when V_{CE} = 1V are greater than the values of V_{BE} when V_{CE}=0V from 5th reading onwards in the tabular column.
   b). The values of V_{BE} when V_{CE} = 2V are greater than the values of V_{BE} when V_{CE}=1V from 5th reading onwards in the tabular column.
9). Plotted the graph between V_{BE} on *X*-axis and I_B on *Y*-axis.
   Note: Do not vary the supply voltage V_{CC} unless V_{BB} is kept at 0 Volts.
10). We did the same experiment in multisim also, and noted down the corresponding values in tabular column (A).

B). Output characteristics :

1). Connected the circuit as shown in the circuit diagram.
2). Now Switched *ON* the *RPS* and all the meters.
3). Kept the I_B = 20µA by varying the supply voltage V_{BB}
4). Varied the supply voltage V_{CC} in steps 0.0V, 0.50V, 1V, 2V, 4.V, 6.V, 8.V, 10V, 15V, 18V, 20V, 22V, 24V, 26V, 28V, 30V and noted down the corresponding readings of V_{CE} and meters.
5). Now kept the V_{CC} at 0V.
6). Repeated the same procedure from steps 4 to 5 for each time independently when I_B=40µA & I_B=40µA which are kept by varying the V_{BB}.
7). Now switched OFF the RPS and all the meters.
8). Took care that ,
   a). The values of I_C when I_B = 40µA are greater than the values of I_C when I_B = 20µA from 5th reading onwards in the tabular column.
   b). The values of I_C when I_B = 40µA are greater than the values of I_C when I_B = 60µA. from 5th reading onwards in the tabular column.
9). Plotted the graph between VC_E on *X*-axis and I_C on *Y*-axis.
   Note: Do not vary the supply voltage V_{BB} unless V_{CC} is kept at 0 Volts.
10). We did the same experiment in multisim also, and noted down the corresponding values in tabular column (B).

TABULAR COLUMNS :

A). Input Characteristics :

Using Hardware : Using Multisim software :

SL. No.	V_{BB} (V)	V_{CE}=0V		V_{CE}=1V		V_{CE}=2V			V_{CE}=0V		V_{CE}=1V		V_{CE}=2V	
		V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)		V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)
1	0.0													
2	0.5													
3	1.0													
4	2.0													
5	4.0													
6	6.0													
7	8.0													
8	10.0													
9	15.0													
10	20.0													
11	25.0													
12	30.0													

B). Output Characteristics :

Using Hardware : Using Multisim software :

SL. No.	V_{CC} (V)	I_B=20µA/ (0.02mA)		I_B=40µA/ (0.04mA)		I_B=60µA/ (0.06mA)			I_B=20µA/ (0.02mA)		I_B=40µA/ (0.04mA)		I_B=60µA/ (0.06mA)	
		V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)		V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)
1	0.0													
2	0.5													
3	1.0													
4	2.0													
5	4.0													
6	6.0													
7	8.0													

--------- In next page will continued ----------

------ **Continued** ------															
SL. No.	**V_{CC} (V)**	**I_B=20µA/ (0.02mA)**		**I_B=40µA/ (0.04mA)**		**I_B=60µA/ (0.06mA)**			**I_B=20µA/ (0.02mA)**		**I_B=40µA/ (0.04mA)**		**I_B=60µA/ (0.06mA)**	
		V_{CE} (V)	**I_C (mA)**	**V_{CE} (V)**	**I_C (mA)**	**V_{CE} (V)**	**I_C (mA)**		**V_{CE} (V)**	**I_C (mA)**	**V_{CE} (V)**	**I_C (mA)**	**V_{CE} (V)**	**I_C (mA)**
8	10.0													
9	15.0													
10	18.0													
11	20.0													
12	22.0													
13	24.0													
14	26.0													
15	28.0													
16	30.0													

EXPECTED GRAPHS :

A). Input characteristics with '*h*' parameters :

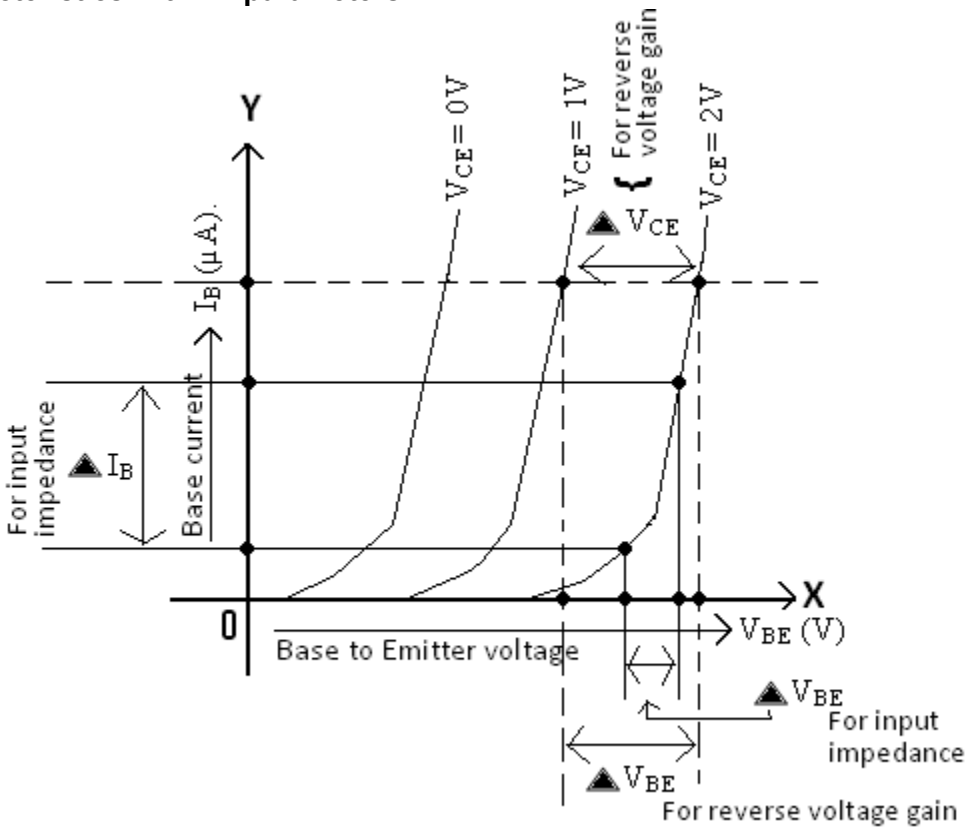


Figure: Measurement of h-parameters of input characteristics in CE configuration.

A). Output characteristics with '*h*' parameters :

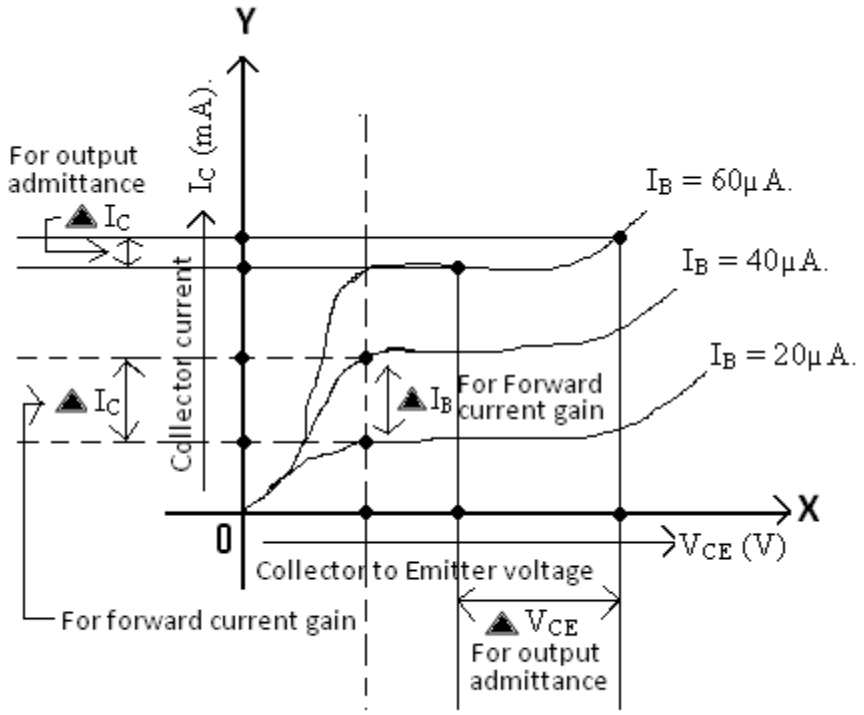


Figure: Measurement of h-parameters of output characteristics in CE configuration.

PARAMETERS :

Common emitter (CE) configuration :

1). Input impedance **(h_{ie})** = $\Delta V_{BE} / \Delta I_B$ = Here V_{CE} is constant.

2). Reverse voltage gain **(h_{re})** = $\Delta V_{BE} / \Delta V_{CE}$ = Here I_B is constant.

Note : The above two parameters are calculated from input characteristics curve of CE configuration.

3). Output admittance **(h_{oe})** = $\Delta I_C / V_{CE}$ = Here I_B is constant.

4). Forward current gain **(h_{fe})** = $\Delta I_C / \Delta I_B$ = Here V_{CE} is constant.

Note : The above two parameters are calculated from output characteristics curve of CE configuration.

5). Forward voltage gain = $1 / h_{re}$. =

6). Output resistance = $1 / h_{oe}$. =

RESULT : The input , output characteristics and '*h*' parameters of a transistor in *Common Emitter configuration* are studied

VIVA VOCE Questions:

1. Define beta DC amplification factors of BJT.

2. Briefly explain reach through effect.

3. Explain the transistor operation with the help of four regions.

4. Compare CB,CE, CC configurations of a transistor.

5. What is the need of biasing?

6. Define stability factor of transistor.

7. What are the advantages of using potential divider bias?

8. Why we use h-parameters to describe a transistor?

9. Mention the characteristics of CE Amplifier.

10. For Amplifier, Transistor operation which region?

Exp. No. Date :

7 BJT CHARACTERISTIC - COMMON BASE (CB) CONFIGURATION

AIM :

To obtain the input and output characteristics of transistor in *Common Base configuration* using Hardware and multisim software.

APPARATUS :

1). Voltmeters :	a). (0 – 2)V	Digital	DC Type	--------- 1 No.
	b). DMM	Digital	DC Type	--------- 1 No.
2). Ammeters	a). (0 – 50)mA	Digital / Analog	DC Type	--------- 1 No.
	b). (0-20)mA	Digital	DC Type	--------- 1 No.
3). Regulated Power Supply (RPS) : Dual channel, (0-30)V, 1A				--------- 1 No.
4). Bread board				--------- 1 No.
5). Connecting wires :				--------- A Few Nos.
6). System with Multisim software				--------- 1 No.

COMPONENTS :

1). Transistor : BC 547	--------- 1 No.
2). Carbon fixed resistors 1 KΩ ,½W	--------- 2 No.

THEORY :

In this configuration we use base as common terminal for both input and output signals. The configuration name itself indicates the common terminal. Here the input is applied between the base and emitter terminals and the corresponding output signal is taken between the base and collector terminals with the base terminal grounded. Here the input parameters are V_{EB} and I_E and the output parameters are V_{CB} and I_C. The input current flowing into the emitter terminal must be higher than the base current and collector current to operate the transistor, therefore the output collector current is less than the input emitter current.

The current gain is generally equal or less than to unity for this type of configuration. The input and output signals are in-phase in this configuration. The amplifier circuit configuration of this type is called as non-inverting amplifier circuit. The construction of this configuration circuit is difficult because this type has high voltage gain values.

The input characteristics of this configuration are looks like characteristics of illuminated photo diode while the output characteristics represents a forward biased diode. This transistor configuration has high output impedance and low input impedance. This type of configuration has high resistance gain i.e. ratio of output resistance to input resistance is high. The voltage gain for this configuration of circuit is given below.

$$A_V = V_{out}/V_{in} = (I_C * R_L) / (I_E * R_{in})$$

Current gain in common base configuration is given as

$$\alpha = \text{Output current/Input current}$$

$$\alpha = I_C/I_E$$

The common base circuit is mainly used in single stage amplifier circuits, such as microphone pre amplifier or radio frequency amplifiers because of their high frequency response. The common base transistor circuit is given below.

CIRCUIT DIAGRAM :

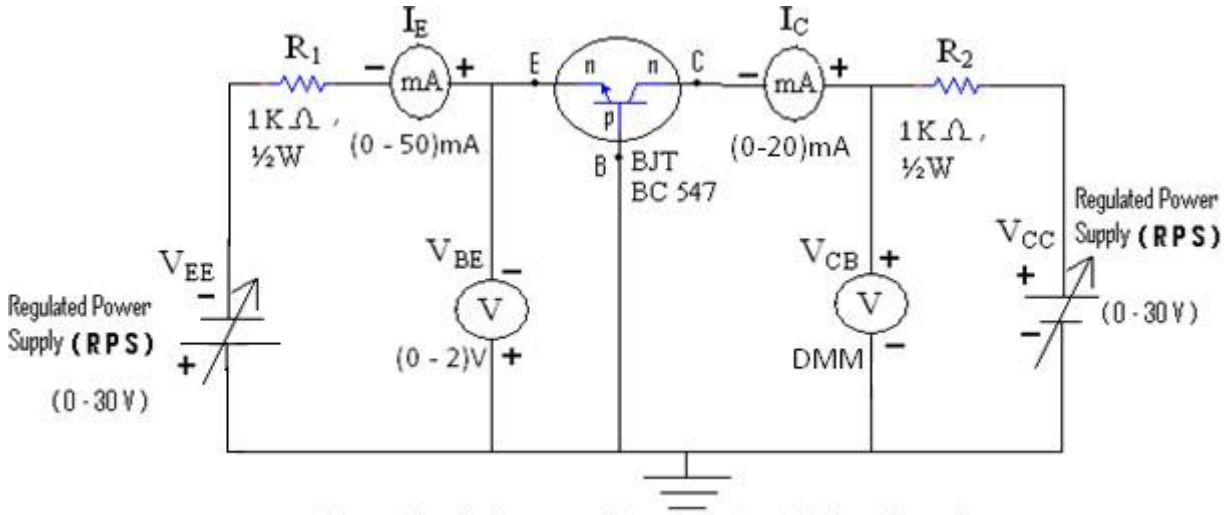


Figure: Circuit diagram of Common Base (CB) configuration.

PROCEDURE :

A). Input characteristics :

1). Connected the circuit as shown in the circuit diagram.

2). Now Switched *ON* the *RPS* and all the meters.

3). Kept the V_{CB} = 0V by adjusted the V_{CC}.

4). Varied the supply voltage V_{EE} in steps of 0V, 0.5V, 1V, 2V, 5V, 10V, 15V, 20V, 25V, 30V and noted down the corresponding readings of V_{BE} and I_E the meters.

5). Kept the V_{EE} at 0V.

6). Repeated the same procedure from steps 4 to 5 for each time independently when V_{CB} = 2V & V_{CB} = 4V by varying the V_{CC}.

7). Now switched OFF the RPS and all the meters.

8). Took care that ,

a). The values of V_{BE} when V_{CB} = 2V are lesser than the values of V_{BE} when V_{CB}=0V from 5th reading onwards in the tabular column.

b). The values of V_{BE} when V_{CB} = 4V are lesser than the values of V_{BE} when V_{CB}=2V from 5th reading onwards in the tabular column.

9). Plotted the graph between V_{BE} on *X*-axis and I_E on *Y*-axis.

Note: *Do not vary the supply voltage V_{CC} unless V_{EE} is kept at 0 Volts.*

10). We did the same experiment in multisim also, and noted down the corresponding values in tabular column (A).

B). Output characteristics :

1). Connected the circuit as shown in the circuit diagram.

2). Now Switched *ON* the *RPS* and all the meters.

3). Kept the I_E = 2mA by varying the supply voltage V_{EE}

4). Varied the supply voltage V_{CC} in steps 0V, 0.5V, 1V, 2V, 5V, 10V, 15V, 20V, 25V, 30Vand noted down the corresponding readings of V_{CB} and $I_C$meters.

5). Now kept the V_{CC} at 0V.

6). Repeated the same procedure from steps 4 to 5 for each time independently when I_E=4mA & I_E=6mA by varying the V_{EE}.

7). Now switched OFF the RPS and allthe meters. 8). Took care that ,

a). The values of V_{CB} when I_E = 4mA are lesser than the values of V_{CB} when I_E = 2mA from 5th reading onwards in the tabular column.

b). The values of V_{CB} when I_E = 6mA are lesser than the values of V_{CB} when I_E = 4mA from 5th reading onwards in the tabular column.

c). The values of I_C when I_E = 4mA are greater than the values of I_C when I_E = 2mA from 5th reading onwards in the tabular column.

d). The values of I_C when I_E = 6mA are greater than the values of I_C when I_E = 4mA from 5th reading onwards in the tabular column.

9). Plotted the graph between V_{CB} on *X*-axis and I_C on *Y*-axis.

Note: *Do not vary the supply voltage V_{EE} unless V_{CC} is kept at 0 Volts.*

10). We did the same experiment in multisim also, and noted down the corresponding values in tabular column (B).

TABULAR COLUMNS :

A). Input Characteristics :

Using Hardware : Using Multisim software :

SL. No.	V_{BB} (V)	V_{CB}=0V		V_{CB}=2V		V_{CB}=4V			V_{CE}=0V		V_{CE}=2V		V_{CE}=4V	
		V_{BE} (V)	I_E (mA)	V_{BE} (V)	I_E (mA)	V_{BE} (V)	I_E (mA)		V_{BE} (V)	I_E (mA)	V_{BE} (V)	I_E (mA)	V_{BE} (V)	I_E (mA)
1	0													
2	0.5													
3	1													
4	2													
5	5													
6	10													
7	15													
8	20													
9	25													
10	30													

B). Output Characteristics :

Using Hardware : Using Multisim software :

SL.No.	V_{CC} (V)	I_E = 2mA		I_E = 4mA		I_E = 6mA			I_E = 2mA		I_E = 4mA		I_E = 6mA	
		V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)		V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)	V_{CB} (V)	I_C (mA)
1	0													
2	0.5													
3	1													
4	2													
5	5													
6	10													
7	15													
8	20													
9	25													
10	30													

EXPECTED GRAPHS :

A). Input Characteristics :

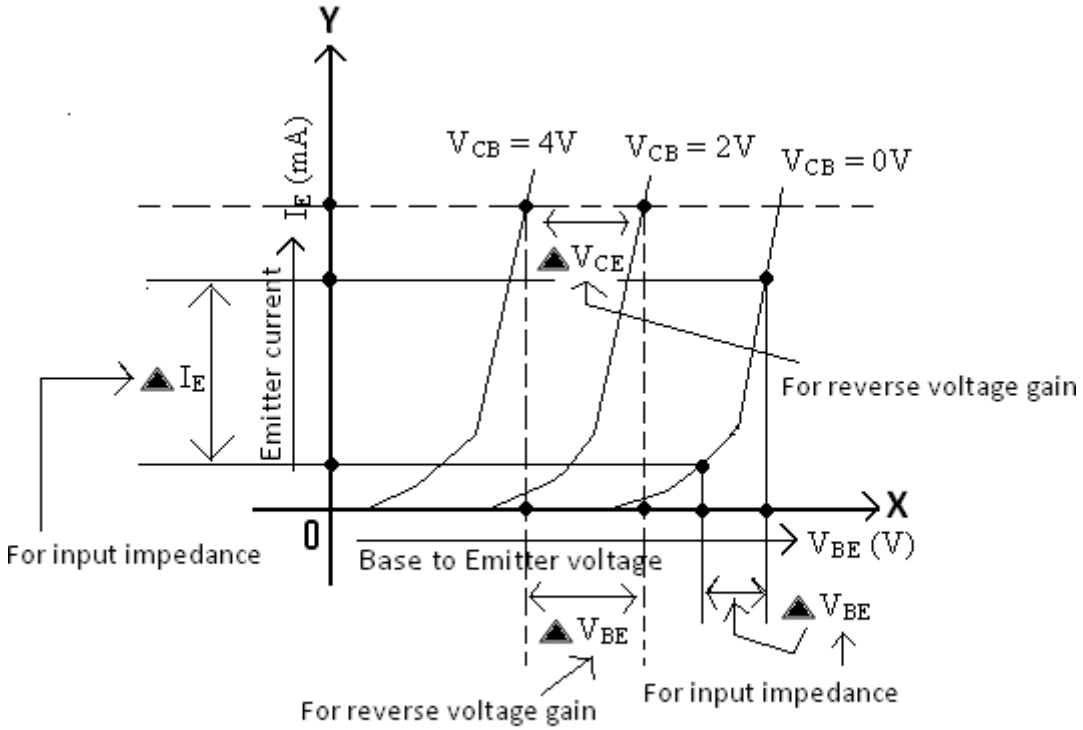


Figure: Measurement of h-parameters of input characteristics in CB configuration.

B). Output Characteristics :

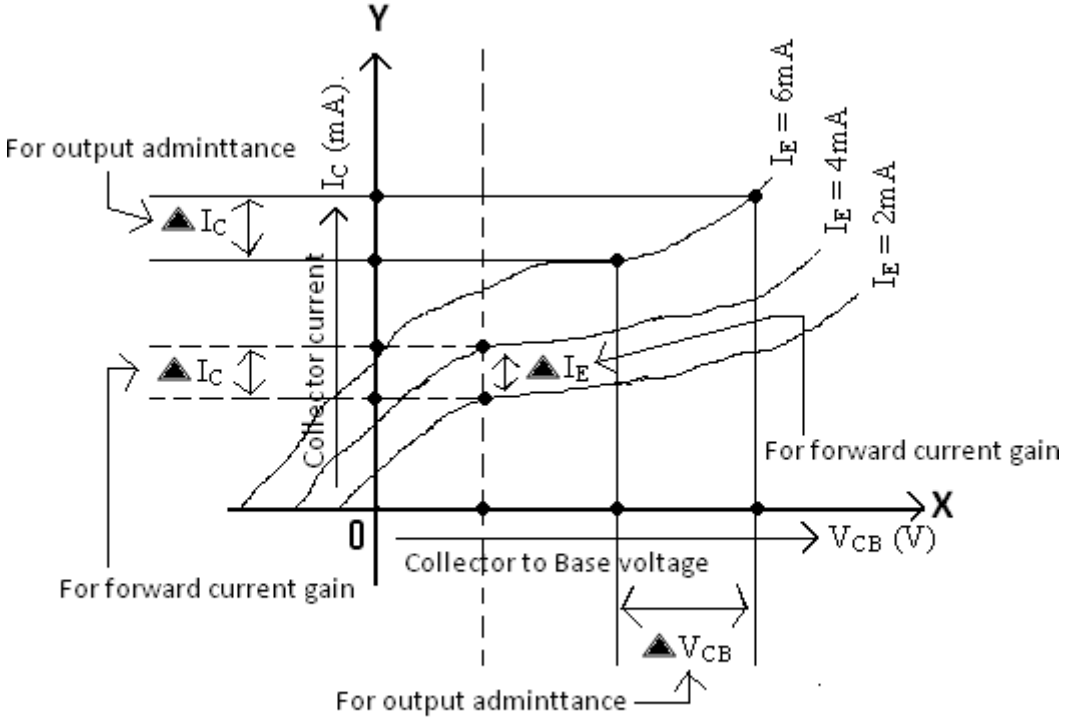


Figure: Measurement of h- parameters of output characteristics in CB configuration.

PARAMETERS :

B). Common base (CB) configuration :

1). Input impedance $(h_{ib}) = \Delta V_{BE} / \Delta I_E$ = Here V_{CB} is constant.
=

2). Reverse voltage gain $(h_{rb}) = \Delta V_{BE} / \Delta V_{CB}$ = Here I_E is constant.

Note : *The above two parameters are calculated from input characteristics curve of CB configuration.*

3). Output admittance $(h_{ob}) = \Delta I_C / V_{CB}$ = Here I_E is constant.

4). Forward current gain $(h_{fb}) = \Delta I_C / \Delta I_E$ = Here V_{CB} is constant.

Note : *The above two parameters are calculated from output characteristics curve of CB configuration.*

5). Forward voltage gain = $1 / h_{rb}$. =

6). Output resistance = $1 / h_{ob}$ =

RESULT :

The input and output characteristics of a transistor in *Common Base configuration* are studied

VIVA VOCE Questions:

1. Mention the characteristics of CB Amplifier.

2. Define alpha DC amplification factors of BJT.

3. Explain the transistor operation with the help of four regions.

4. Compare CB, CE, CC configurations of a transistor.

5. What is the need of biasing?

6. Define stability factor of transistor.

7. What are the advantages of using potential divider bias?

8. Why we use h-parameters to describe a transistor?

9. For Amplifier, Transistor operation which region?

10. Briefly explain reach through effect.

Exp. No. 8 Date :

UNI JUNCTION TRANSISTOR (UJT) CHARACTERISTICS

AIM :

1). To draw the volt ampere / static characteristics of ***UJT*** using Hardware as well as Multisim software
2). To determine the *Intrinsic stand of ratio (η), Peak current (I_P), Valley current (I_V) , Peak voltage (V_P) , Valley Voltage (V_V)*

APPARATUS :

1) Regulated Power Supply (RPS):		(0-30)V	Dual Channel		---- 1 No.
2) Voltmeters	:	(0-10)V	Analog	DC Type	---- 1No.
3) Ammeters	:	(0-20)mA	Digital	DC Type	---- 1 No.
4) Bread board	:				---- 1 No.
5) Connecting wires	:			----	A few Nos.
6) System with multisim software	:				---- 1No.

COMPONENTS :

1). UJT 2N2646	:				---- 1No.
2). Resistors 1/2W	:	2.2KΩ			---- 1No.

THEORY :

A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. It has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is opencircuit is called interbase resistance. The original UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length.

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits. When the emitter voltage reaches Vp, the current starts to increase and the emitter voltage starts to decrease.

CIRCUIT DIAGRAM :

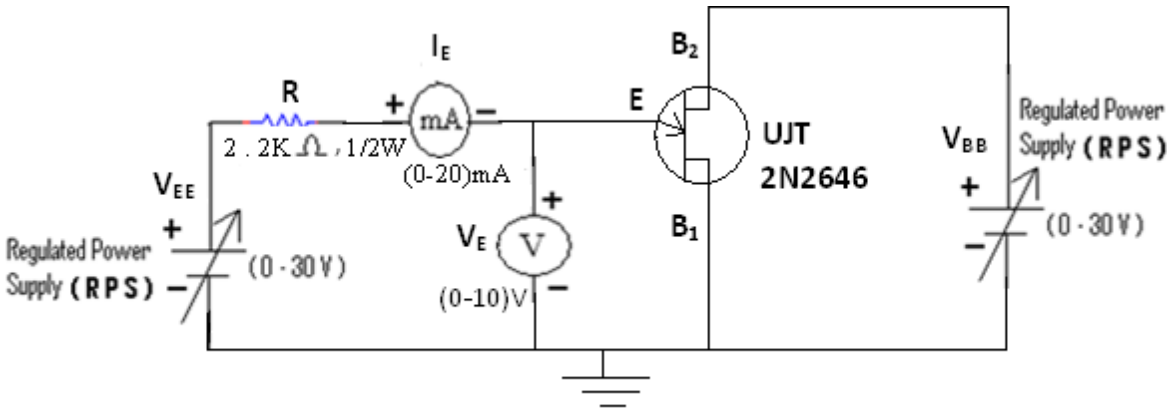


Figure: Circuit diagram of Unijunction transistor characteristics.

PROCEDURE :

1). Connections are made as per the circuit diagram.
2). Kept the **V_{BB}** at **4V** by varying the **V_{BB}** i.e. Regulated Power Supply(RPS).
3). By varied the V_{EE} I observed that in V_E at one certain peak (max.) point it is suddenly fallen and noted the two readings of V_{EE}, V_E, I_E at which the V_E is falling just from its maximum point & after the fallen, in the table form-1.
4). Now Kept the V_{EE} at 0V.
5). By varied the **V_{EE}** in steps i.e 0V, 2.6V, 2.7V, 2.8V, 2.9V, 3.0V, 5.5V, 5.6V, 5.7V, 5.8V, 5.9V,6.0V, 6.2V, 6.4V, 10V, 20V, 30V I have noted down the corresponding readings of **V_E** & **I_E** into the tabular form-2.
6). Inserted the readings which are available in tabular form-1 into the tabular form-2 in ascendingorder.
7). After completed of taken the readings, kept the **V_{EE}** at **0V**.
8). Now I have kept the **V_{BB}** at **8V**olts by varying **V_{BB}** i.e. Regulated Power Supply(RPS).
9). Repeat the same steps from 3 to 7 .
10). After completed of taken the readings, kept the **V_{EE}** & **V_{BB}** at **0V**.
11). Finally switched **OFF** the RPS and all meters.
12). Plotted the graph by taken the Emitter current **I_E** on **X** – axis and Emitter voltage **V_E** on **Y**- axis using the readings in tabular form – 2.
13). Calculated the *Negative resistance* and *Intrinsic stand of ratio* from the graph, according to the formulas, which are given under the heading of **PARAMETERS**
14). We did the same experiment using multisim software , noted down the corresponding values in the tabular form 1&2.

TABULAR FORM - 1 :

Using Hardware : Using Software :

Heading	V_{BB} = 4 Volts			V_{BB} = 8 Volts				V_{BB} = 4 Volts			V_{BB} = 8 Volts		
	V_{EE} in volts	V_E in Volts	I_E in mA	V_{EE} in volts	V_E in Volts	I_E in mA		V_{EE} in volts	V_E in Volts	I_E in mA	V_{EE} in volts	V_E in Volts	I_E in mA
1. Just before the max point at which suddenly fallen in V_E													
2. Just after fallen from max. point in V_E													

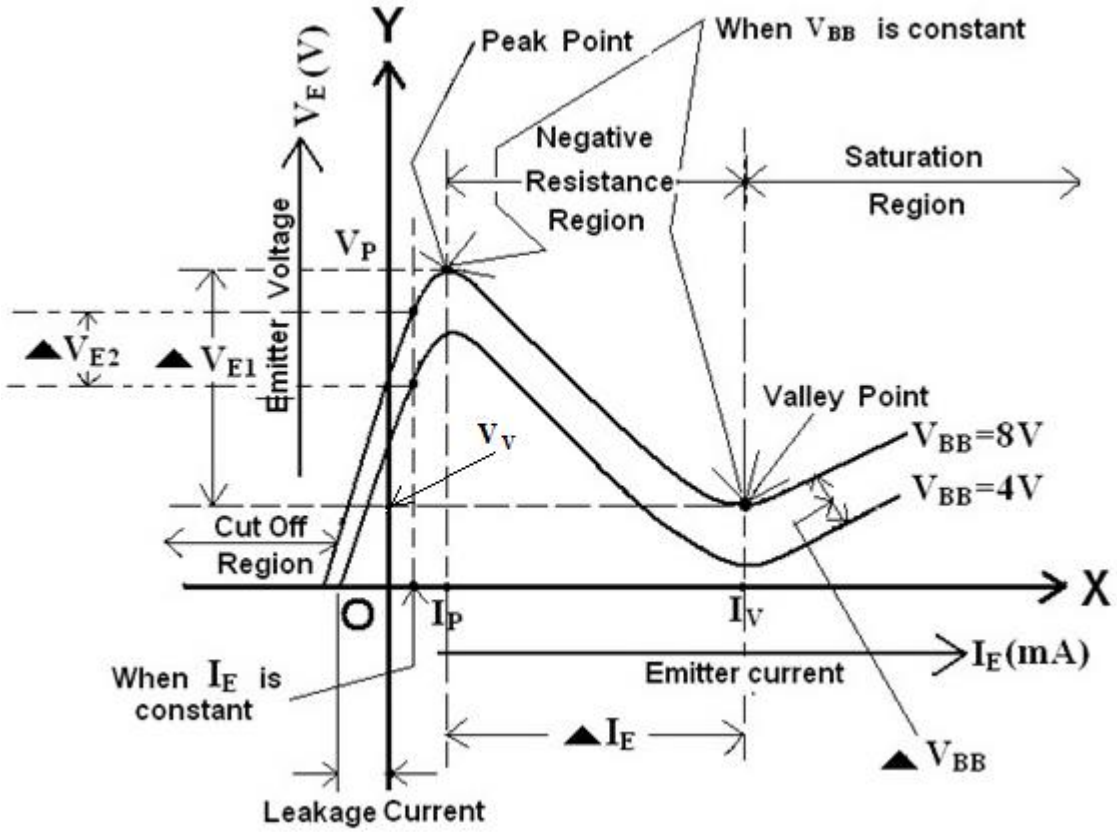
TABULAR FORM - 2 :

Using Hardware : Using Multisim Software :

Sl. No.	V_{BB} = 4 Volts			V_{BB} = 8 Volts				V_{BB} = 4 Volts			V_{BB} = 8 Volts		
	V_{EE} in volts	V_E in Volts	I_E in mA	V_{EE} in volts	V_E in Volts	I_E in mA		V_{EE} in volts	V_E in Volts	I_E in mA	V_{EE} in volts	V_E in Volts	I_E in mA

EXPECTED GRAPH :

The following graph shows for ***Uni junction Transistor Characteristics.***



PARAMETERS :

1. Negtive resistance $= \dfrac{\triangle V_{E1}}{\triangle I_E}$ When, V_{BB} is constant

2. Intrinsic stand off ratio $\eta = \dfrac{\triangle V_{E2}}{\triangle V_{BB}}$ When, I_E is constant

Note: The typical value of ***Intrinsic stand off ratio*** is 0.51 to 0.82

3. Peak current I_P =
4. Valley current I_V =
5. Peak Voltage V_P =
6. Valley Voltage V =

RESULT :

We have drawn the graph for volt ampere characteristics of *Unijunction Transistor.*

VIVA VOCE Questions:

1. What is UJT?

2. Which device used in relaxation oscillators?

3. UJT operating in which resistive region?

4. Mention the UJT Applications.

5. What is the intrinsic standoff ratio?

6. Mention typical value of intrinsic standoff ratio.

7. P-side Emitter in UJT is_____doped. (heavily or lightly)

8. When Emitter terminal of UJT is open then the resistance of the base terminal is _____ (very high or very low).

9. How many terminals are there in a UJT?

10. Which type of material is the channel

Exp. No. 9 Date :

SILICON CONTROLED RECTIFIER (SCR) CHARACTERISTICS

AIM :

To draw the Volt Ampere characteristics of ***SCR*** using Hardware as well as in Multisim software

APPARATUS :

1). SCR Trainer kit				------	1 No.
2). Voltmeters	:	(0-20)V	Digital	------	2 No.
3). Ammeters	:	(0-200)mA	Digital/Analog	------	1 No.
		(0-2000)µA	Digital	------	1 No.
4). DMM	:		Digital	------	1 No.
5). Connecting wires :				------	A few Nos.
6). System with Multisim software				------	1 No.

THEORY :

Thyristor Characteristics:- A thyristor is a four layer semiconductor device of PNPN structure with three PN junctions. It has three terminal anode, cathode and gate. When the anode voltage is made positive with respect to cathode, the junctions J1 and J3 are forward biased. The junctions J2 is reversed biased and, only a small leakage current flows from anode to cathode. The thyristor is then said to be in the OFF mode. If a Anode to Cathode voltage is increased to a sufficiently large value, the reversed biased junction J2 will break. This is known as avalanche breakdown and the corresponding voltage is called forward breakdown voltage VBO. Since junctions J1 and J3 are already forward biased, there will be free movement of carriers across all three junctions, resulting in a large forward anode current. The device will then be in a conducting state or on state. The voltage drop would be due to the ohmic drop in the four layers and it is small, typically, 1V. In the on state, the anode current is limited by an external impedance or resistance.

Latching current is the minimum anode current required to maintain the thyristor in the on state immediately after the thyristor has been turned on and the gate signal has been removed. Once the thyristor is turned on, it behaves like a conducting diode and there is no control over the device. The device will continue to conduct because there is no depletion layer on the junction J2 due to the free movements of the carriers. However if the forward anode current is reduced below a level known as the holding current, a depletion layer will develop around the junction J2, due to reduced number of carriers and the thyristor will be in the blocking state. Holding current is the minimum anode current required to maintain the thyristor in the on state. Holding current is less than latching current. A thyristor can be turned on by increasing the forward voltage VAK beyond VBO, but such a turn on could be destructive. In practice, the forward voltage is maintained below VBO and the thyristor is turned on by applying a positive voltage between its gate and cathode. Once a thyristor is turned on by a gating signal and its anode current is greater than holding current, the device continues to conduct due to positive feedback, even if the gating signal is removed.

CIRCUIT DIAGRAM :

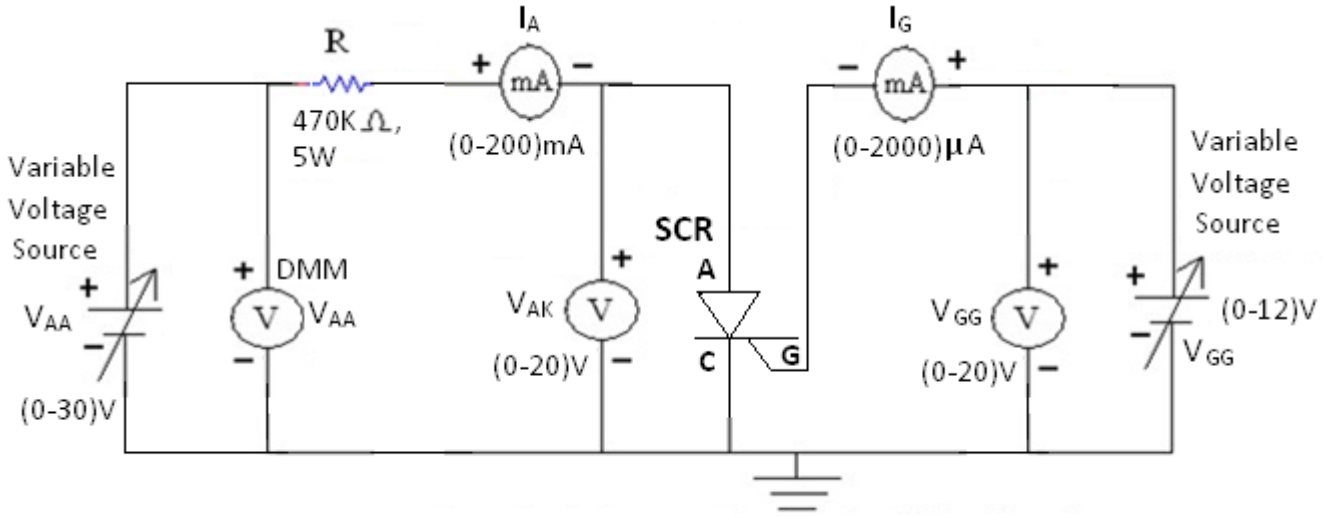


Figure : Circuit diagram of SCR Characteristics

TABULAR COLUMN :

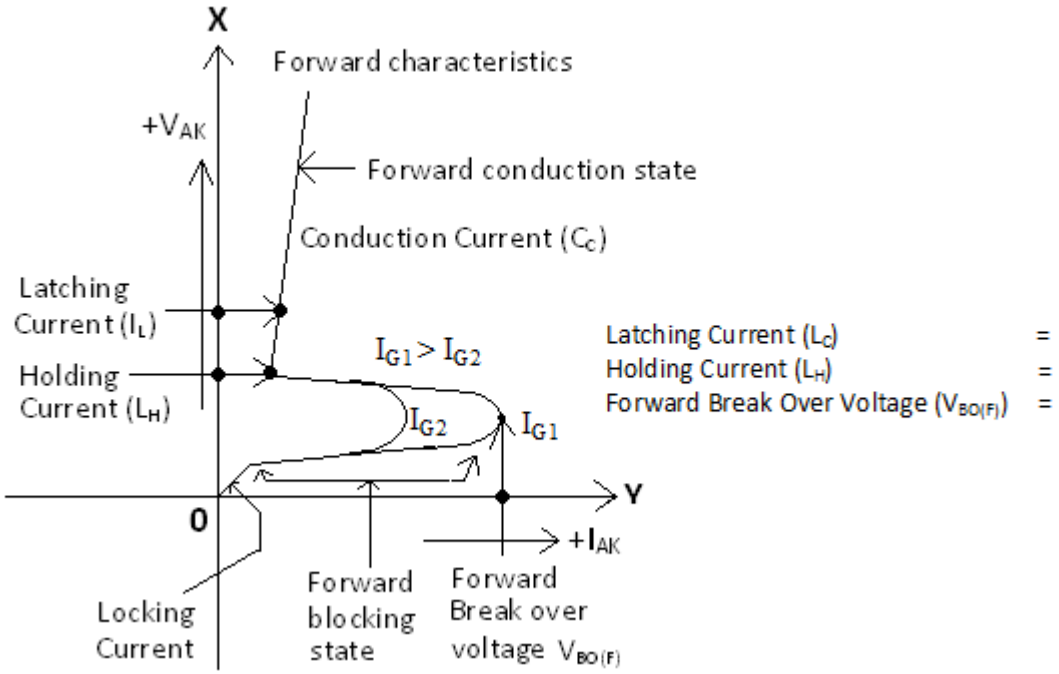
Using Hardware : Using Multisim Software :

	When V_{AK} = 2V						When V_{AK} = 2V				
Sl. No.	V_{AA} In Volts	V_{AK} In Volts	I_A In mA	I_G In μA	V_{GG} In Volts		V_{AA} In Volts	V_{AK} In Volts	I_A In mA	I_G In μA	V_{GG} In Volts
1	0.00										
4	2.00	2.00					2.00	2.00			
5											
6											
7											
8											
9											
10											
11											
12											

PROCEDURE :

1). We connected the circuit as per shown in the tabular column.
2). By kept V_{AA} as 0V and 2V noted down the corresponding readings in the corresponding columns of the tabular column. But at these values there is no value in I_A & I_G meters.
3) Now we varied the V_{GG} until the Anode current slightly varied and noted this value in the tabular column.
4). Again varied the V_{GG} until the Anode current largly varied and noted this value in the tabular column.
5). Now Stopped the V_{GG} to vary, now varied the V_{AA} in the steps of 10V, 20V, 30V and noted down the corresponding values in the tabular column.
6). We observed that when V_{AA} increases I_A also increases but at last suddenly the I_A is decreased.
7). Took the I_{AK} on X-axis and V_{AK} on Y-axis. Drawn the graph as per values in the tabular column. From that graph found the Latching current, Holding current, Forward Break over Voltage.
8). By kept V_{AA} as 0V and 4V noted down the corresponding readings in the corresponding columns of the tabular column. But at these values there is no value in I_A & I_G meters.
9). Repeated the above procedure from steps 3 to 7.
10). We did the same experiment in the *Multisim* software also, and noted down the corresponding values in the corresponding columns of tabular column.

EXPECTED GRAPH :



RESULT : We studied the V-I characteristics of SCR and found the values for the following parameters,

Latching Current (L_C) =
Holding Current (L_H) =
Forward Break Over Voltage ($V_{BO(F)}$) =

VIVA VOCE Questions:

1. What is the characteristics of SCR ?

2. What is the working principle of SCR ?

3. How SCR is started and stopped ?

4. How many junctions are in SCR ?

5. What is switching characteristics of SCR during turn On ?

6. What are dynamic characteristics of SCR ?

7. What are the conditions to turn ON an SCr ?

8. How does the SCR differ from an ordinary rectifier?

9. When a SCR is conducting it has?

10. Why is SCR always turned on by gate current?

Exp. No. 10 Date :

VOLTAGE DIVIDER BIAS CIRCUIT USING BJT

AIM :

1). To design the *Voltage divider bias circuit using BJT* in Hardware and Multisim software.

APPARATUS :

1). Regulated power supply (RPS)	:(0-30)V, 1A	Dual channel		------	1 No.
2). Ammeter	:(0-2000)µA	Digital	DC Type	------	1 No.
	(0-20)mA	Digital	DC Type	------	2 No.
3). Digital Multi Meter (DMM)	:	Digital		------	1 No.
4). Bread Board	:			------	1 No.
5). Connecting wires	:			------	A few Nos.
6). System with Multisim software	:			------	1 No.

COMPONENTS :

1). Resistors 1/2W	:	100 Ω, 3.3 KΩ , 10 KΩ , 100KΩ	------	Each 1 No.
2). Bipolar Junction Transistor (BJT):		BC547-npn	------	1 No.

THEORY :

Voltage divider bias is the most popular and used way to bias a transistor. It uses a few resistors to make sure that voltage is divided and distributed into the transistor at correct levels.

Voltage divider biasing is commonly used why? - Quora. Because Voltage divider biasing is beta-independent and hence is more stable than any other biasing. The temperature will have no effect on Q-point. Also as Voltage divider biasing always operates in the Active region, it's more commonly used.

Another configuration that can provide high bias stability is voltage divider bias. Instead of using a negative supply off of the emitter resistor, like two-supply emitter bias, this configuration returns the emitter resistor to ground and raises the base voltage.

The resistors help to give complete control over the voltage and current that each region receives in the transistor. And the emitter resistor, RE, allows for stability of the gain of the transistor, despite fluctuations in the β values.

The disadvantage of using high value resistors in a voltage divider is it makes the output impedance higher and hence makes the output voltage more sensitive to loading. Lets run some approximate numbers. At audio frequencies we can regard a coaxial cable as a capacitor.

Voltage divider bias is the most popular and used way to bias a transistor. It uses a few resistors to make sure that voltage is divided and distributed into the transistor at correct levels. One resistor, the emitter resistor, RE also helps provide stability against variations in β that may exist from transistor to transistor.

Design : Design a voltage divider bias circuit using Si NPN transistor having $\beta = 360$, $V_{CC} = 10V$, $V_{CE} = 6V$, $V_{BE} = 0.75$, $I_C = 1$ mA

a). I_B I_E & V_E :

$$I_B = \frac{I_C}{\beta} = \frac{1\times10^{-3}}{360} = 2.77\mu A$$

$$I_E = I_B + I_C = 2.77\times10^{-6} + 1\times10^{-3}$$

$$= (0.00277+1)\times10^{-3} = 1\text{ mA}$$

$$\boxed{I_E = 1\text{ mA}}$$

$$V_E = \frac{V_{CC}}{100} = \frac{10}{100} = 0.1V$$

b). R_E & R_C :

$$R_E = V_E / I_E = 0.1V / 1\times10^{-3}$$

$$\boxed{R_E = 100\,\Omega}$$

Apply KVL to collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{10 - 6 - 0.1}{1\times10^{-3}}$$

$$\boxed{R_C = 3.9K\,\Omega \simeq 3.3K\,\Omega}$$

C). R_1 & R_2 :

$$V_B = V_E + V_{BE} = 0.1V+0.7V = 0.8V$$

$$I_{R1} = I + I_B \qquad I_{R2} = I$$

$$I = 30 I_B = 30\times2.77\times10^{-6} = 83.1\mu A$$

$$R_2 = V_B / I = 0.8/83\times10^{-6}$$

$$\boxed{R_2 = 9.63K\,\Omega \simeq 10K\,\Omega}$$

$$R_1 = \frac{V_{CC} - V_B}{I + I_B} = \frac{10\text{-}0.8}{(83.1\times10^{-6} + 2.77\times10^{-6})}$$

$$R_1 = \frac{(9.2\times1000)}{85.87}\times10^3 = 107K\,\Omega$$

$$\boxed{R_1 \simeq 100K\,\Omega}$$

d). R_B & S :

Thevenins resistance $R_B = \frac{R_1 \times R_2}{R_1 + R_2}$

$$R_B = \frac{100\times10^3\times10\times10^3}{(100\times10^3)+(10\times10^3)} = \frac{1000}{110}\times10^3$$

$$R_B = 9.09K\,\Omega \simeq 9K\,\Omega$$

$$\text{Stability factor } S = 1+\beta\left[\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}}\right]$$

$$S = 1+360\left[\frac{1+\frac{9\times10^3}{100}}{1+360+\frac{9\times10^3}{100}}\right] = 361\left[\frac{10^3(0.1+9)}{100}\times\frac{100}{10^3(36.1+9)}\right]$$

$$\boxed{S = 361\times0.201 = 72.561}$$

CIRCUIT DIAGRAM :

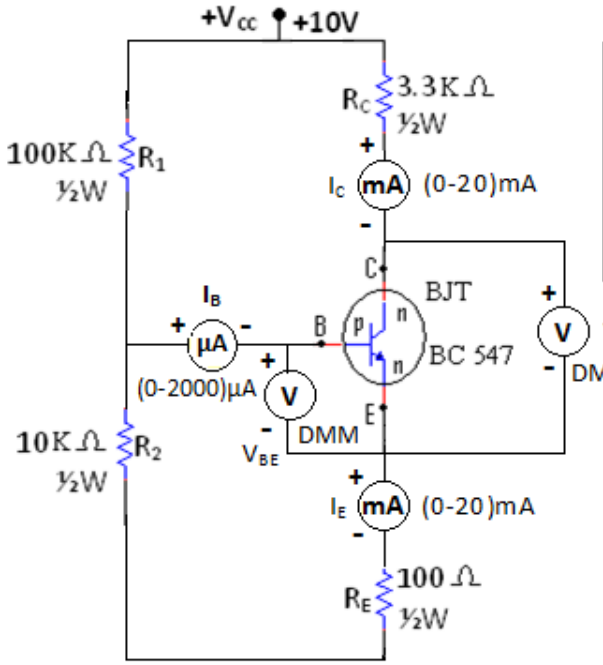


Figure: Circuit for Voltage divider bias using BJT

TABULAR COLUMN :

Using Hardware

Sl. No	V_{CC} (V)	V_{BE} (V)		V_{CE} (V)		I_C (mA)		I_E (mA)		I_B (µA)	
		T. Value	P. Value	T Value	P. Value	T. Value	P. Value	T. Value	P. Value	T. Value	P. Value
----	----										
1	10	0.75		6		1		1		3	

Using Multisim

Sl. No	V_{CC} (V)	V_{BE} (V)		V_{CE} (V)		I_C (mA)		I_E (mA)		I_B (µA)	
		T. Value	P. Value	T Value	P. Value	T. Value	P. Value	T. Value	P. Value	T. Value	P. Value
----	----										
1	10	0.75		6		1		1		3	

PROCEDURE :

1). Connected the circuit as per shown in the circuit diagram.
2). Kept the RPS at 10V as V_{CC}
3). Noted down the corresponding values in the tabular column which are shown in meters.
4). By Compared the theoretical and practical values both are same approximately .
5). Kept the RPS at 0V and switched off all the meters.
6). Repeated the same procedure in Multisim software also, and noted down the the corresponding values in the tabular column

RESULT :

Designed the voltage divider bias circuit using the BJT in Hardware as well as in Multisim software.

VIVA VOICE Questions:

1. What is need for biasing?

2. Define stability factor of transistor.

3. What are the advantages of using potential divider bias?

4. What is the difference between bias compensation and stabilization?

5. List out the Biasing Techniques.

6. Alternative names of Voltage Divider Bias?

7. Applications of Voltage Divider Bias?

8. How much value of Stability factor for Voltage Divider Bias?

9. What is the Thevenin's Theorem?

10. Compare Self Bias with Fixed Bias, Collector to base bias.

Exp. No. 11 Date :

VOLTAGE DIVIDER BIAS CIRCUIT USING JFET

AIM :

1). To design the *Voltage divider bias circuit using JFET* in Hardware and Multisim software.

APPARATUS :

1). Regulated power supply (RPS)	:(0-30)V, 1A	Dual channel		------	1 No.
2). Ammeter	:(0-20)mA	Digital	DC Type	------	1 No.
3). Digital Multi Meter (DMM)	:	Digital		------	1 No.
4). Bread Board	:			------	1 No.
5). Connecting wires	:			------	A few Nos.
6). System with Multisim software	:			------	1 No.

COMPONENTS :

1). Resistors 1/2W	:	1.8KΩ, 100KΩ	------	Each 1 No.
	:	2.2 KΩ	------	2 No.
2). Junction Field Effect Transistor (JFET)	:	BF W11	------	1 No.

THEORY :

Two series connected resistors form a voltage divider circuit. ... In this way, the applied drain voltage is **utilized to get** the gate terminal voltage. A resistance is inserted into source terminal in series. The device current flows through the resistance and causes a voltage

The JFET Amplifier

Just like the bipolar junction transistor, JFET's can be used to make single stage class A amplifier circuits with the JFET common source amplifier and characteristics being very similar to the BJT common emitter circuit. The main advantage JFET amplifiers have over BJT amplifiers is their high input impedance which is controlled by the Gate biasing resistive network formed by R1 and R2 as shown.

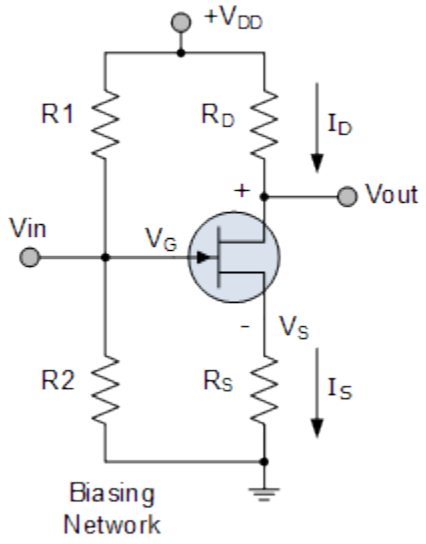
Biasing of JFET Amplifier

$$V_S = I_D R_S = \frac{V_{DD}}{4}$$

$$V_S = V_G - V_{GS}$$

$$V_G = \left(\frac{R2}{R1+R2}\right)V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$



This common source (CS) amplifier circuit is biased in class "A" mode by the voltage divider network formed by resistors R1 and R2. The voltage across the Source resistor R_S is generally set to be about one quarter of V_{DD}, (V_{DD} /4) but can be any reasonable value.
The required Gate voltage can then be calculated from this R_S value. Since the Gate current is zero, ($I_G = 0$) we can set the required DC quiescent voltage by the proper selection of resistors R1 and R2.
The control of the Drain current by a negative Gate potential makes the **Junction Field Effect Transistor** useful as a switch and it is essential that the Gate voltage is never positive for an N-channel JFET as the channel current will flow to the Gate and not the Drain resulting in damage to the JFET. The principals of operation for a P-channel JFET are the same as for the N-channel JFET, except that the polarity of the voltages need to be reversed.

In the next tutorial about **Transistors**, we will look at another type of Field Effect Transistor called a *MOSFET* whose Gate connection is completely isolated from the main current carrying channel.

Design : Design a N channel BFW11 JFET circuit which is provided by Voltage divider bias as per following data

V_{DD} = 10V, V_{DS} = 8V, V_P = -6V , I_D = 1 mA, I_{DSS} = 10 mA. This is the data sheet of BF W11 JFET.

$$I_D = I_{DSS}\left[1-\frac{V_{gs}}{V_p}\right]^2$$

$$1\times10^{-3} = 10\times10^{-3}\left[\frac{-(6+V_{gs})}{-6}\right]^2$$

$$\frac{1\times10^{-3}}{1\times10^{-3}} = \frac{(6+V_{gs})^2}{36}$$

$$0.1\times36 = (6+V_{gs})^2$$

$(6+V_{gs})^2$ Is in the form of $(a+b)^2$

so it can written as (a^2+b^2+2ab)

$$3.6=36+V_{gs}^2+12V_{gs}$$

$$\boxed{1V_{gs}^2+12V_{gs}+32.4=0}$$

The above equation in the form of $ax^2+bx+c=0$ So, a=1, b=12, c=32.4 the roots of this equation can find by using the following formula,

$$x=\frac{-b\pm\sqrt{b^2-4ac}}{2a}$$

$$V_{gs}=\frac{-12\pm\sqrt{(12)^2-4\times1\times32.4}}{2\times1}$$

$$=\frac{-12+3.79}{2}=-4.105$$

$$=-12-3.79 = -7.895$$

V_{gs} = -4.105 **OR** -7.895

As per problem, V_{DS} =8V. If we Would like to operate JFET in Saturation region, then then the Following condition should satisfy, $V_{DS}>Vgs - V_P$ & V_{DS} should +ve value.

So we substituted -4.105 & 6 in the form $V_{DS}>Vgs - V_P$,

8 > -4.105-(-6)

8 > +1.895V

Now we substituted -7.895& 6 in the form $V_{DS}>Vgs- V_P$,

8 > -7.895-(-6)

8 > -1.895V

So here the $\boxed{V_{gs} = -4.105}$

$$R_D = \frac{V_{DD}-V_{DS}}{I_D} = \frac{10-8}{1\times10^{-3}} = 2\ K\Omega$$

$\boxed{\text{Choose } R_D = 2.2K}$

$V_S = I_D R_S$

$1.8=1\times10^{-3}\times R_S$

$$R_S = \frac{1.8}{1\times10^{-3}} = 1.8K\Omega$$

$\boxed{R_S = 1.8K\Omega}$

$$V_{GG} = \frac{R_2}{R_1+R_2}\times V_{DD}$$

$$0.215 = \frac{R_2}{102.2\times10^3}\times10$$

$$R_2 = \frac{0.215\times102.2\times10^3}{10} = 2.2K\Omega$$

$\boxed{\text{Choose } R_2 = 2.2K\Omega}$

As per problem R_1+R_2=102.2K

$R_1 = R_2 - 2.2K = 100K\Omega$

Choose R_1 = 100KΩ

CIRCUIT DIAGRAM :

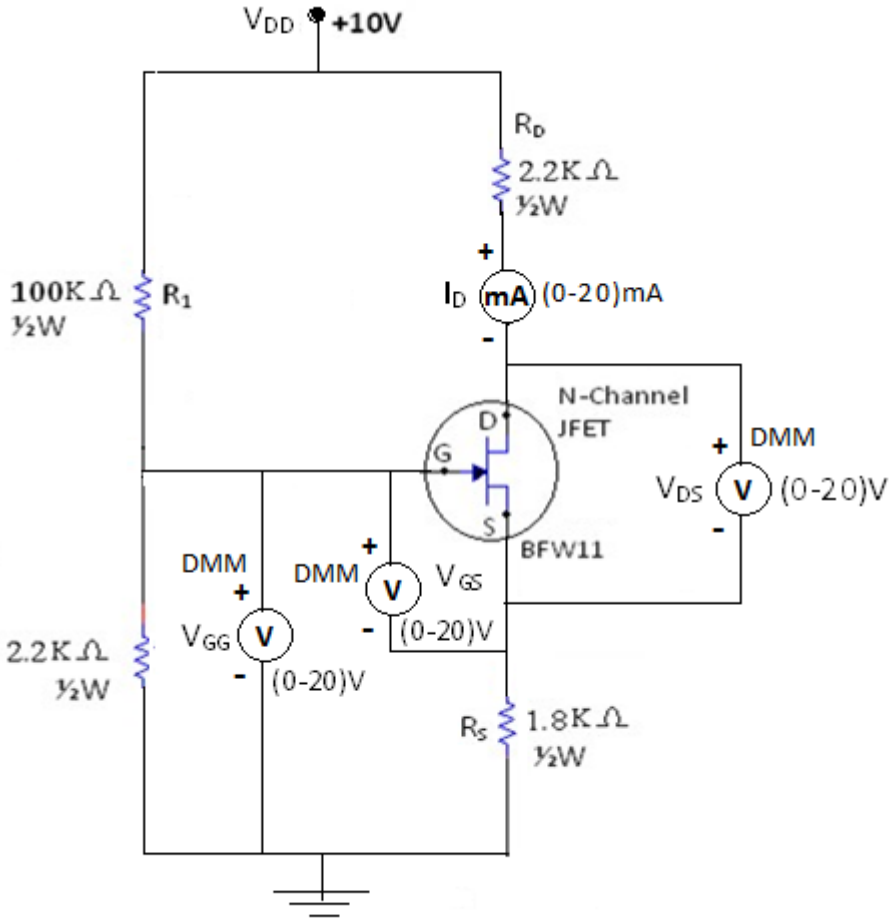


Fig : Circuit diagram for Voltage divider bias using JFET

PROCEDURE :

1). Connected the circuit as per shown in the circuit diagram.
2). Kept the RPS at 10V as V_{DD}
3). Noted down the corresponding values in the tabular column which are shown in meters.
4). By Compared the theoretical and practical values both are same approximately .
5). Kept the RPS at 0V and switched off all the meters.
6). Repeated the same procedure in Multisim software also, and noted down the the corresponding values in the tabular column

TABULAR COLUMN :

Using Hardware :

Sl. No	V_{DD} (V)	V_{DS} (V)		V_{GG} (V)		V_{GS} (V)		I_D (mA)	
		T. Value	P. Value	T. Value	P. Value	T. Value	P. Value	T. Value	P. Value
1	10	8		0.215				1	

Using Multisim software :

Sl. No	V_{DD} (V)	V_{DS} (V)		V_{GG} (V)		V_{GS} (V)		I_D (mA)	
		T. Value	**P. Value**	**T. Value**	**P. Value**	**T. Value**	**P. Value**	**T. Value**	**P. Value**
1	10	8		0.215				1	

RESULT :

Designed the voltage divider bias circuit using the JFET in Hardware as well as in Multisim software.

VIVA VOCE Questions:

1. What is need for biasing?

2. Define stability factor of transistor.

3. What are the advantages of using potential divider bias?

4. Compare voltage divide bias for BJT and FET.

5. List out the Biasing Techniques.

6. Alternative names of Voltage Divider Bias?

7. Applications of Voltage Divider Bias?

8. How much value of Stability factor for Voltage Divider Bias?

9. What is the Thevenin's Theorem?

10. Compare Self Bias with Fixed Bias, Collector to base bias.

Exp. No. 12	Date :

BJT AS A SWITCH

AIM :

To design the Switch with self bias using BJT.

APPARATUS :

1). Regulated power supply (RPS)	:(0-30)V, 1A	Dual channel		------	1 No.
2). Ammeter	:(0-2000)µA	Digital	DC Type	------	1 No.
	:(0-20)mA	Digital	DC Type	------	1 No.
3). Digital Multi Meter (DMM)	:	Digital		------	1 No.
4). Bread Board	:			------	1 No.
5). Connecting wires	:			------	A few Nos.
6). System with Multisim software	:			------	1 No.

COMPONENTS :

1). Resistors 1/2W	:	1KΩ, 400KΩ, 1MΩ	------	Each 1 No.
2). Bipolar Junction Transistor (BJT)	:	BC547-npn	------	1 No.
3). Buzzer	:		------	1 No.

THEORY :

Bipolar junction transistor (BJT) has three terminals and two junctions. The function of the transistor is to amplify the signal. The three terminals of BJT are base, emitter and collector. BJT is either a PNP transistor or NPN transistor based on the doping type of the three terminals. Using the transistor as a switch is the simplest application of transistors.

How does a BJT act as a switch? A transistor has three modes: active region, cut off region and the saturation region. The transistor acts as a switch in the cut-off mode and the saturation mode. The transistor is fully off in the cutoff region and fully on the saturation region. A transistor can also be used as a switch since a small electric current flowing through one part of it can cause larger current flow through the other part of the transistor.

Design : Design a suitable circuit for switch using BJT, to ON buzzer. The data sheet of Buzzer is given below,

V_{CCmax} = 12V, I_C = 4mA, V_{BE} = 0.75V, β or h_{FE} = 360.

Sol :

$I_C = \beta I_B$

$I_B = I_C / \beta = (4\times10^{-3})/360$

$I_B = 11.11\mu A$

$$R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{5-0.75}{11.11\times10^{-6}}$$

$R_B = 382K\Omega$

Choose $R_B = 400K\Omega$

→ In the formula $R_B = \frac{V_{BB} - V_{BE}}{I_B}$

decreased. if R_B increases, I_B decreases

then in $I_C = \beta . I_B$ if β is constant I_B decreases then I_C is decreased.

→ If we followed to the above condition,

select $R_B >>> 400K$, I choosed R_B = 1M, Now,

$$R_B = \frac{V_{BB} - V_{BE}}{I_B} \Rightarrow \frac{1\times10^6}{1} = \frac{4.25}{I_B}$$

$$I_B = \frac{4.25}{1\times10^6} \Rightarrow \boxed{I_B = 4.25\mu A}$$

$I_C = \beta . I_B \Rightarrow I_C = 360\times4.25\times10^{-6}$

$\boxed{I_C = 1.53mA}$

→ As per our problem to switched ON Buzzer I_C should 4mA, But if R_B =1M ,then we got I_C = 1.5mA. So this current value could not sufficient. At this condition the buzzer could switched OFF.

CIRCUIT DIAGRAM :

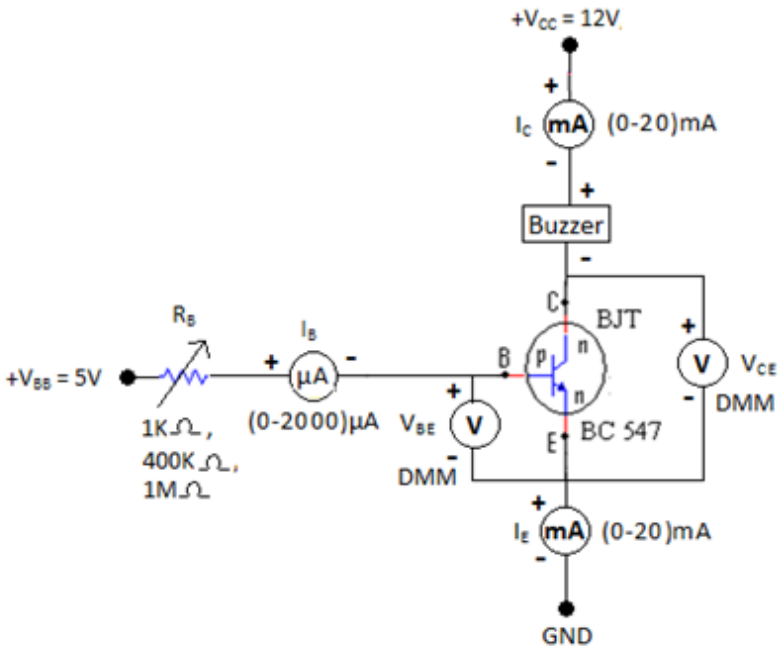


Figure : Circuit diagram of a switch using BJT

PROCEDURE :

1). Connected the circuit as per shown in the circuit diagram.
2). Kept the RPS at 12V as V_{CC}.
3). Kept R_B =1KΩ and noted down the corresponding values in the tabular column.
4). Repeated the above procedure from step 2 to step 3 for R_B = 400KΩ and 1MΩ.
5). Observed that, at R_B = 1KΩ and 400KΩ the BJT is biased why because the V_{BE} >=0.75V and the I_C value is more at R_B =1KΩ as compared to R_B =400KΩ . At these two conditions the Buzzer is switched ON.

6). But BJT didn't bias at R_B = 1MΩ why because the V_{BE} <0.75V and I_C=1.53mA. This current would not sufficient to switched ON the Buzzer.

7). Repeated the same procedure in Multisim software also, and noted down the the corresponding values in the tabular column

TABULAR COLUMN :

Using Hardware : Using Multisim Software :

Sl.No.	R_B in Ω	V_{BE} in Volts	V_{CE} in Volts	I_C in Volts	I_E in Volts	I_B in Volts		V_{BE} in Volts	V_{CE} in Volts	I_C in Volts	I_E in Volts	I_B in Volts
01	1KΩ											
02	400KΩ											
03	1MΩ											

RESULT :

I have designed the Switch with self bias using BJT.

VIVA VOCE Questions:

1. In which Region Transistor act as Switch? (Active or saturation or cut-off)

2. When Base current is zero, Then Transistor act as_____(Switch off or switch on).

3. What is Early effect in BJT?

4. Compare BJT switch and FET switch.

5. Explain the transistor operation with the help of four regions.

6. What is the Cut- In-Voltage of Transistor?

7. Classification of Transistors.

8. Mention the Transistor applications.

9. What is the importance of biasing in Transistors?

10. Compare CB,CE, CC configurations of a transistor.

Exp. No. 13 Date :

HALF WAVE RECTIFIER

(Beyond the Syllabus)

AIM :

1). To study the characteristics of *Half wave rectifier with and without filter* using Software and HArdware
2). To obtain the ripple factor and percentage of regulation of this same.

APPARATUS :

1). Voltmeter :	(0 – 20)V	Digital / Analog	DC Type	-----	1 No
2). Ammeters :	(0 – 500)mA	Digital / Analog	DC Type	-----	1 No.
3). Digital Multi Meter (DMM)				-----	1 No.
4). Decade Resistance Box (DRB)				-----	1 No.
5). Cathode Ray Oscilloscope (CRO)				-----	1 No.
6). Probes				-----	2 No.
7). Bread board				-----	1 No.
8). Connecting wires :				-----	A few Nos

COMPONENTS :

1). PN Diode 1N4007		-----	1 No.
2). Electrolytic capacitor (Filter)	i). 100µF, 25V	-----	1 No.
ii). 1000µF,25V	----- 1No.		
3). Centre tapped step down transformer	12-0-12V, 500mA	-----	1 No.

THEORY :

A simple Half Wave Rectifier is nothing more than a single pn junction diode connected in series to the load resistor. As you know a diode is to electric current like a one-way valve is to water, it allows electric current to flow in only one direction. This property of the diode is very useful in creating simple rectifiers which are used to convert AC to DC.

When a single rectifier diode unit is placed in series with the load across an ac supply, it converts alternating voltage into a uni-directional pulsating voltage, using one-half cycle of the applied voltage, the other half cycle being suppressed because it conducts only in one direction. Unless there is an inductance or battery in the circuit, the current will be zero, therefore, for half the time. This is called ***half-wave rectification***. As already discussed, a diode is an electronic device consisting of two elements known as cathode and anode. Since in a diode electrons can flow in one direction only *i.e.* from the cathode to anode, the diode provides the unilateral conduction necessary for rectification. This is true for diodes of all types-vacuum, gas-filled, crystal or semiconductor, metallic (copper oxide and selenium types) diodes. Semiconductor diodes, because of their inherent advantages are usually used as a rectifying device. However, for very high voltages, vacuum diodes may be employed.

Applications :

1. They are used for signal demodulation purpose
2. They are used for rectification applications
3. They are used for signal peak applications

Disadvantages :

1. Power loss
2. Low output voltage
3. The output contains a lot of ripples

CIRCUIT DIAGRAMS :

A).Half wave rectifier without Filter :

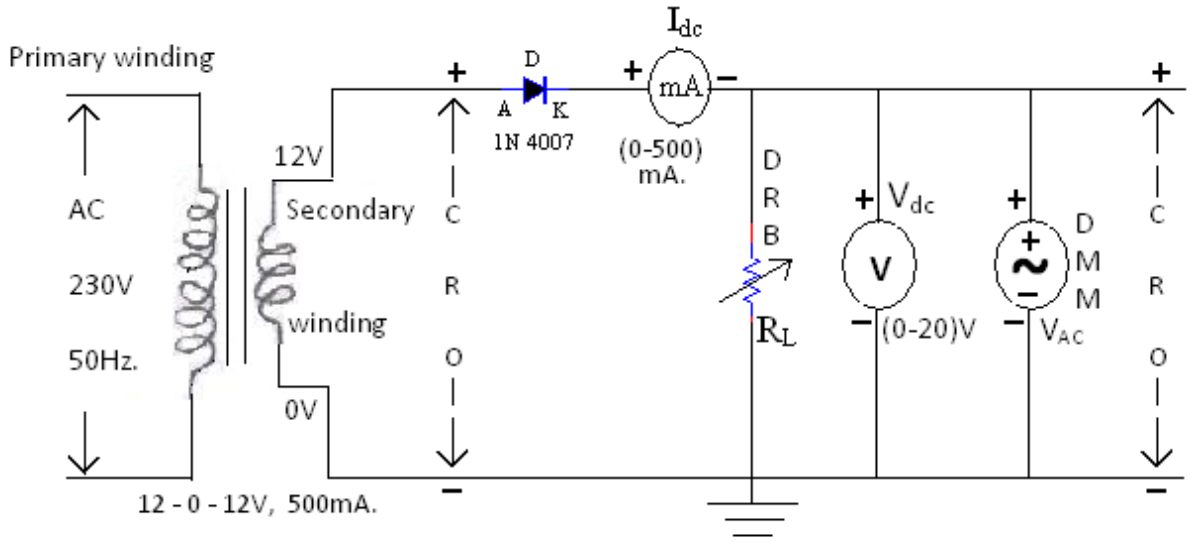


Figure: Circuit diagram of Half wave rectifier without filter.

B). Half wave rectifier with 100µF&1000µF Filter (Capacitor) :

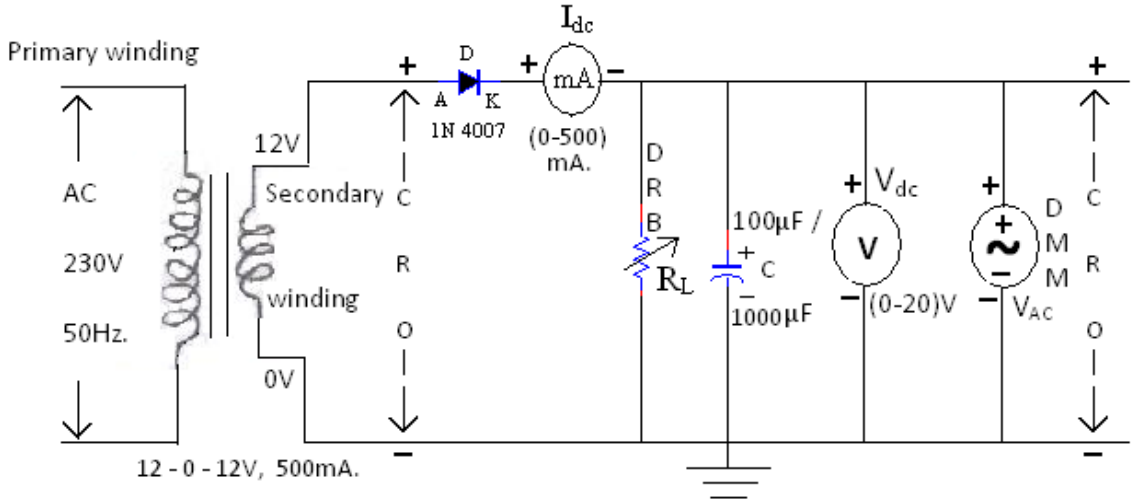


Figure: Circuit diagram of Half wave rectifier with filter using 100µF & 1000µF capacitors.

PROCEDURE :

A). Half wave rectifier without Filter :

1). Connected the circuit as shown in the circuit diagram.
2). Connected the channel1's probe of CRO across the secondary winding and channel2's probe of CRO across the output (DMM) side (as per shown in the circuit) to observe the input sine wave form and output signal respectively.
3). Removed the Decade resistance box (DRB) i.e. load resistance(R_L) from the circuit.
4). Then switched ON the transformer, and all the meters in the circuit,but don't switched ON the CRO.
5). Noted down the No load DC voltage(V_{NL}) in the given specified tabular form from the DMM.
6). After that kept the 100Ω resistance value in the DRB.
7). Now reconnected the DRB to the circuit.
8). Varied the DRB in steps of 100Ω, 500Ω, 1KΩ, 20KΩ, 40KΩ, 60KΩ, 80KΩ, 90KΩ and noted down the values of DC Current (I_{dc}), DC voltage(V_{dc}), AC voltage(V_{AC}) from the corresponding meters.

9). Took care about that DRB always is not at 0Ω resistance value while taking the readings otherwise components and instruments connected in the circuit may get damage.
10). Now kept the DRB at standard resistance value of 1KΩ.
11). Then switched ON the CRO.
12). Kept the *AC/GND/DC* switch of channel1 is at *AC* position and channel2 is at *DC* position.
13). Now kept the *channel position* switch of CRO is at dual mode.
14). Plotted the input sine wave (which is at secondary side & available in channel1) and output signal (which is across DMM & available in channel2) on single graph sheet by observing in the *CRO*.
15). Now switched OFF the transformer, CRO and all the meters in the circuit.
16). Calculated the ripple factor(RF) and % of load regulation by using the for given below,

$$RF = V_{ac} / V_{dc} \quad \text{and \% of load regulation} = \left[\frac{V_{NL}- V_L}{V_L}\right] \times 100$$

17). Plotted the graphs as per below,
a). DC current (I_{dc}) on X-axis and Ripple factor(RF) on Y-axis.
b). DC current (I_{dc}) on X-axis and % of regulation Y-axis.

18). We did the same in the Multisim software and noted down the corresponding values in the tabular column.
19). We compared the Hardware & Software values.

B). Half wave rectifier with 100μF&1000μF Filter (Capacitor):

1). Connected the circuit by using 100μF filter (capacitor) as shown in the circuit diagrams.
2). Connected the channel1's probe of CRO across the secondary winding and channel2's probe of CRO across the output (DMM) side (as per shown in the circuit) to observe the input sine wave form and output signal respectively.
3). Removed the Decade resistance box (DRB) i.e. load resistance(R_L) from the circuit.
4). Then switched ON the transformer, and all the meters in the circuit.
5). But don't switched ON the CRO.
6). Noted down the No load DC voltage(V_{NL}) in the given specified tabular form from the DMM.
7). After that kept the 100Ω resistance value in the DRB.
8). Now reconnected the DRB to the circuit.
9). Varied the DRB in steps of 100Ω, 500Ω, 1KΩ, 20KΩ, 40KΩ, 60KΩ 80KΩ, 90KΩ, and noted down the values of DC Current (I_{dc}), DC voltage(V_{dc}), AC voltage(V_{AC}) from the corresponding meters.
10). Took care about that DRB always is not at 0Ω resistance value while taking the readings otherwise components and instruments connected in the circuit may get damage.
11). Now kept the DRB at standard resistance value of 1KΩ.
12). Then switched ON the CRO.
13). Kept the *AC/GND/DC* switch of channel1 is at *AC* position and channel2 is at *DC* position.
14). Now kept the *channel position* switch of CRO is at dual mode.
15). Plotted the input sine wave (which is at secondary side & available in channel1) and output signal (which is across DMM & available in channel2) on single graph sheet by observing in the *CRO*.
16). Now switched OFF the transformer, CRO and all the meters in the circuit.
17). Then disconnected the 100μF capacitor and reconnect the 1000μF in the same place.
18). Repeated the same procedure from step 3 To step 15.
19). Calculated the ripple factor(RF) and % of load regulation for 100μF and 1000μF by using the formulas given below,

$$RF = V_{ac} / V_{dc} \quad \text{and \% of load regulation} = \left[\frac{V_{NL}- V_L}{V_L}\right] \times 100$$

20). Drawn the following 4 graphs for each time when 100µF and 1000µF capacitors are connected, (It means 4 graphs when 100µF and another 4 graphs when 1000µF capacitors are connected).
   a). DC current (I_{dc}) on X-axis and Ripple factor(RF) on Y-axis.
   b). DC current (I_{dc}) on X-axis and % of regulation Y-axis.
   c). Load resistance(R_L) on X-axis and Ripple Factor (RF) on Y-axis.
   d). Load resistance(R_L) on X-axis and % of Load regulation (RF) on Y-axis.

21) We did the same in the Multisim software and noted down the corresponding values in the tabular column.

22 We compared the Hardware & Software values.

TABULAR COLOUMNS :

A). Half wave rectifier without Filter using Software :

	No Load dc voltage (V_{NL}) = In volts					
Sl. No.	**Load Resistance R_L Ω/KΩ**	**DC current (I_{dc}) in mA.**	**DC voltage (V_{dc} / V_L) in Volts.**	**AC voltage (V_{ac}) in Volts.**	**Ripple Factor (R_F) = V_{ac}/V_{dc}**	**% Of Regulation** $=\left[\frac{V_{NL}-V_L}{V_L}\right]\times 100$
1.	100Ω					
2.	500Ω					
3.	1KΩ					
4.	20KΩ					
5.	40KΩ					
6.	60KΩ					
7.	80KΩ					
8.	90KΩ					

B). Half wave rectifier without Filter using Hardware :

	No Load dc voltage (V_{NL}) = In volts					
Sl. No.	**Load Resistance R_L Ω/KΩ**	**DC current (I_{dc}) in mA.**	**DC voltage (V_{dc} / V_L) in Volts.**	**AC voltage (V_{ac}) in Volts.**	**Ripple Factor (R_F) = V_{ac}/V_{dc}**	**% Of Regulation** $=\left[\frac{V_{NL}-V_L}{V_L}\right]\times 100$
1.	100Ω					
2.	500Ω					
3.	1KΩ					
4.	20KΩ					
5.	40KΩ					
6.	60KΩ					
7.	80KΩ					

C). Half wave rectifier with 100µF capacitor filter using Software :

	No Load dc voltage (V_{NL}) = _____ In volts.						
Sl. No.	**Load Resistance (R_L) In Ω/KΩ**	**DC current (I_{dc}) in mA.**	**DC voltage (V_{dc}/ V_L) InVolts.**	**AC voltage (V_{ac}) in Volts.**	**Theoretical Ripple Factor (R_F) = $\frac{1}{2\sqrt{3}(F \times C \times R_L)}$**	**Practical Ripple Factor(R_F) =V_{ac}/V_{dc}**	**% Of Regulation $= \left[\frac{V_{NL}-V_L}{V_L}\right] \times 100$**
1.	100Ω						
2.	500Ω						
3.	1KΩ						
4.	20KΩ						
5.	40KΩ						
6.	60KΩ						
7.	80KΩ						
8.	90KΩ						

D). Half wave rectifier with 100µF capacitor filter using Hardware :

	No Load dc voltage (V_{NL}) = _____ In volts.						
Sl. No.	**Load Resistance (R_L) In Ω/KΩ**	**DC current (I_{dc}) in mA.**	**DC voltage (V_{dc}/ V_L) InVolts.**	**AC voltage (V_{ac}) in Volts.**	**Theoretical Ripple Factor (R_F) = $\frac{1}{2\sqrt{3}(F \times C \times R_L)}$**	**Practical RippleFactor (R_F)=V_{ac}/V_{dc}**	**% Of Regulation $= \left[\frac{V_{NL}-V_L}{V_L}\right] \times 100$**
1.	100Ω						
2.	500Ω						
3.	1KΩ						
4.	20KΩ						
5.	40KΩ						
6.	60KΩ						
7.	80KΩ						
8.	90KΩ						

E). Half wave rectifier with 1000μF capacitor filter using Software :

	No Load dc voltage (V_{NL}) = _____ In volts.						
Sl. No.	**Load Resistance (R_L) In Ω/KΩ**	**DC current (I_{dc}) in mA.**	**DC voltage (V_{dc}/ V_L) InVolts.**	**AC voltage (V_{ac}) in Volts.**	**Theoretical Ripple Factor (R_F) = $\frac{1}{2\sqrt{3}(F \times C \times R_L)}$**	**Practical Ripple Factor(R_F) =V_{ac}/V_{dc}**	**% Of Regulation $= \left[\frac{V_{NL}-V_L}{V_L}\right] \times 100$**
1.	100Ω						
2.	500Ω						
3.	1KΩ						
4.	20KΩ						
5.	40KΩ						
6.	60KΩ						
7.	80KΩ						
8.	90KΩ						

F). Half wave rectifier with 1000μF capacitor filter using Hardware :

	No Load dc voltage (V_{NL}) = _____ In volts.						
Sl. No.	**Load Resistance (R_L) In Ω/KΩ**	**DC current (I_{dc}) in mA.**	**DC voltage (V_{dc}/ V_L) InVolts.**	**AC voltage (V_{ac}) in Volts.**	**Theoretical Ripple Factor (R_F) = $\frac{1}{2\sqrt{3}(F \times C \times R_L)}$**	**Practical RippleFactor (R_F)=V_{ac}/V_{dc}**	**% Of Regulation $= \left[\frac{V_{NL}-V_L}{V_L}\right] \times 100$**
1.	100Ω						
2.	500Ω						
3.	1KΩ						
4.	20KΩ						
5.	40KΩ						
6.	60KΩ						
7.	80KΩ						
8.	90KΩ						

EXPECTED WAVEFORMS (Half wave rectifier) :

A). Without Filter :

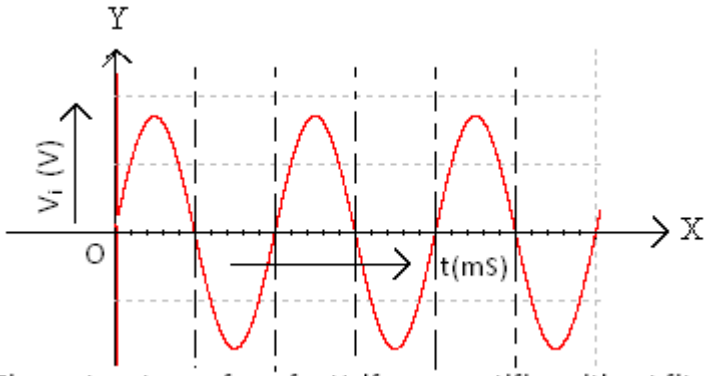


Figure: Input waveform for Half wave rectifier without filter

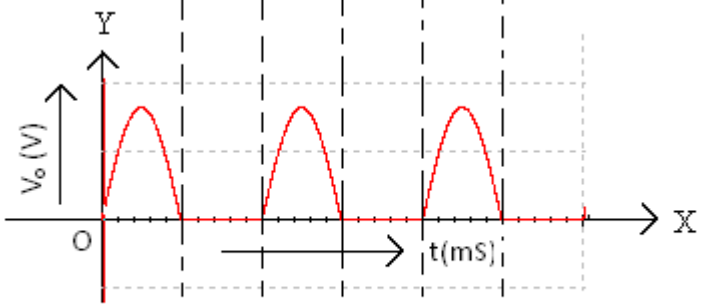


Figure: Output waveform for Halfwave rectifier without Filter at R_L=1 KΩ

B). With 100µF Filter (capacitor), at R_L=1KΩ :

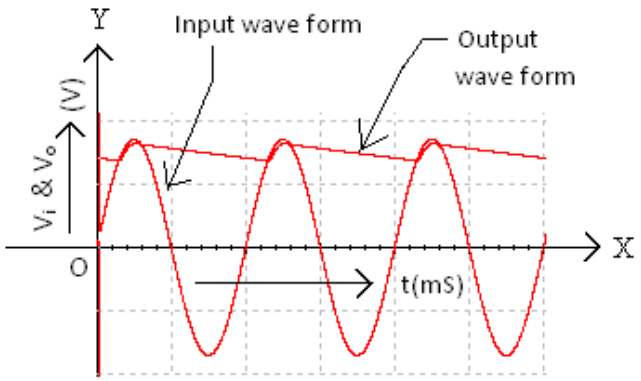


Figure: Input & output waveform for Half wave rectifier when 100µF filter(capacitor) is connected at R_L=1 KΩ

C). With 1000µF Filter (capacitor), at R_L=1KΩ :

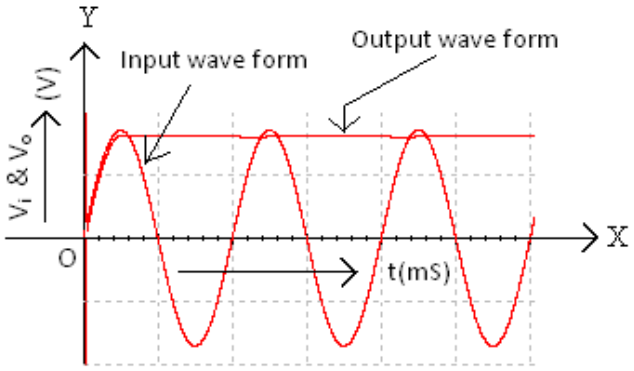
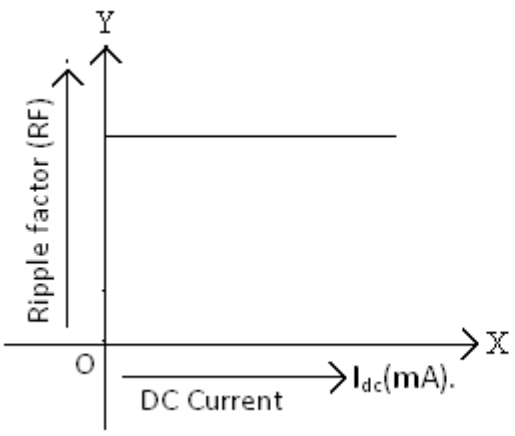
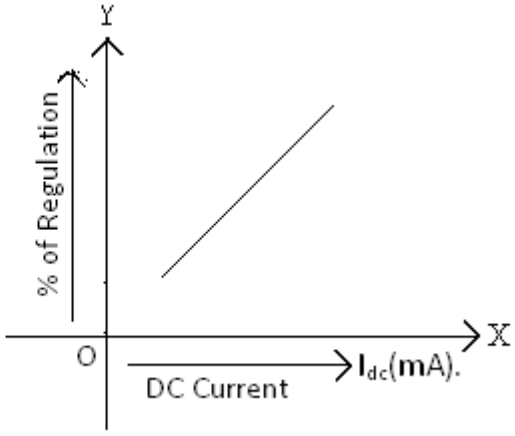


Figure: Input & output waveform for Half wave rectifier when 1000 µF filter(capacitor) is connected at R_L=1 KΩ

EXPECTED GRAPHS (Half wave rectifier):

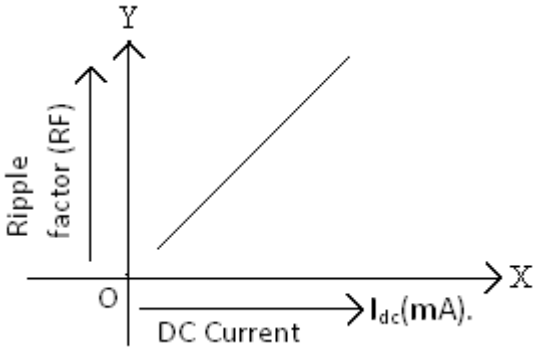
A). Without Filter :

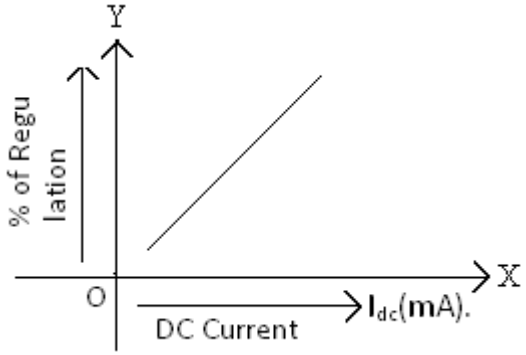


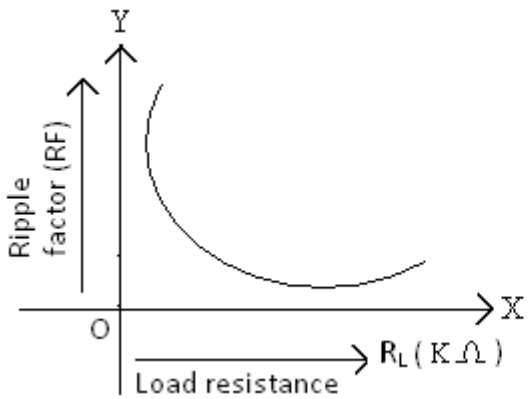


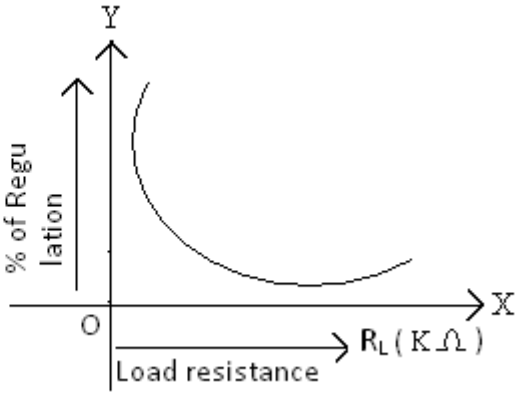
B). With 100µF & 1000µF Filter (capacitor) :

Note: Drawn the separate graph sheets for 100µF & 1000µF capacitors. i.e 4 graphs for 100µF and another 4 graphs for 1000µF capacitors as per given below,









PARAMETERS (Half wave rectifier):

THEORETICAL VALUES	PRACTICAL VALUES
A). Without Filter: Ripple factor (RF) = 1.1	Ripple factor (RF) when R_L is at 1KΩ = *(Noted down from the tabular column).*
B). With 100μF capacitor: Ripple factor (RF) = $\frac{1}{2\sqrt{3}(F \times C \times R_L)}$ Where, F = 50Hz., C=100μF, R_L=1KΩ	Ripple factor (RF) when R_L is at 1KΩ = *(Noted down from the tabular column).*
C). With 1000μF capacitor: Ripple factor (RF) = $\frac{1}{2\sqrt{3}(F \times C \times R_L)}$ Where, F = 50Hz., C=1000μF, R_L=1KΩ	Ripple factor (RF) when R_L is at 1KΩ = *(Noted down from the tabular column).*

RESULT :

A). Without filter:

We studied the characteristics of *Half wave rectifier without filter and* obtained the ripple factor , % of regulation at R_L=1KΩ. The values are given below,

1). Ripple factor(RF) =
2). % of regulation =

B). With 100μF & 1000μF filter (capacitor) :

We studied the characteristics of *Half wave rectifier with filter* and obtained the ripple factor , % of regulation at R_L=1KΩ., The values are given below,

1). Ripple factor(RF) for 100μF =
2). % of regulation for 100μF =
3). Ripple factor(RF) for 1000μF =
4). % of regulation for 1000μF =

VIVA VOCE Questions:

1. What is Rectifier?

2. Classification of Rectifiers.

3. What is the Ripple Factor of HWR?

4. What is TUF of HWR?

5. HWR consists of how many diodes?

6. Mention the applications of Rectifier.

7. What is the Efficiency of HWR?

8. What is the Peak factor of HWR?

9. What is the function of filter in Rectifiers?

10. Mention the properties of L and C components.

Exp. No. 14

Date :

Voltage Doubler Circuit

(Beyond the Syllabus)

AIM :

1). To study the characteristics of *Half wave rectifier with and without filter* using Software and HArdware
2). To obtain the ripple factor and percentage of regulation of this same.

APPARATUS :

1). Cathode Ray Oscilloscope (CRO)	-----	1 No.
2). Function generator (FG)	-----	1 No.
3). Probes	-----	2 No.
4). Bread board	-----	1 No.
5). Connecting wires :	-----	A few Nos

COMPONENTS :

1). PN Diode 1N4007		-----	2 No.
2). Electrolytic capacitor (Filter)	i). 100µF, 25V	-----	2 No.

THEORY :

The circuit intakes an input voltage and multiplies it by 2 to give an output voltage that is 2 times larger than the input voltage. Thus, this circuit is a type of voltage multiplier circuit.

The circuit intakes an AC voltage signal and outputs a larger DC voltage signal. Thus, the circuit is a type of AC-to-DC converter, an AC-to-DC boost

The capacitors we use all all 100µF electrolytic capacitors. Lower values can be used, such as 20-50µF, but these are hard to find, so we simply use 100µF, but you can experiment with this.

CIRCUIT DIAGRAM :

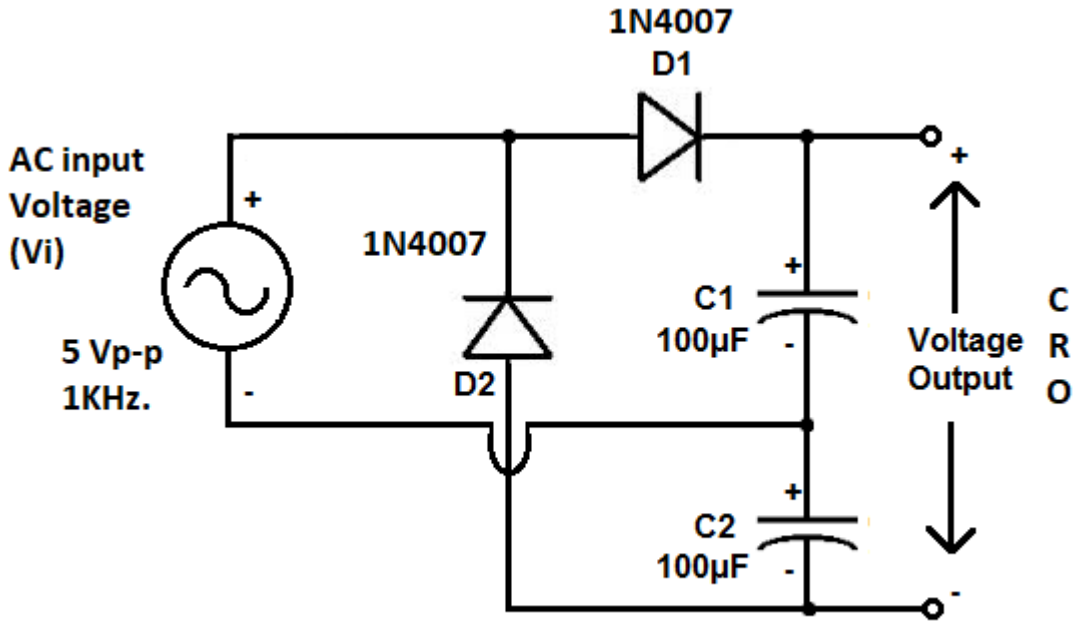


Fig : Voltage Doubler Ckt.

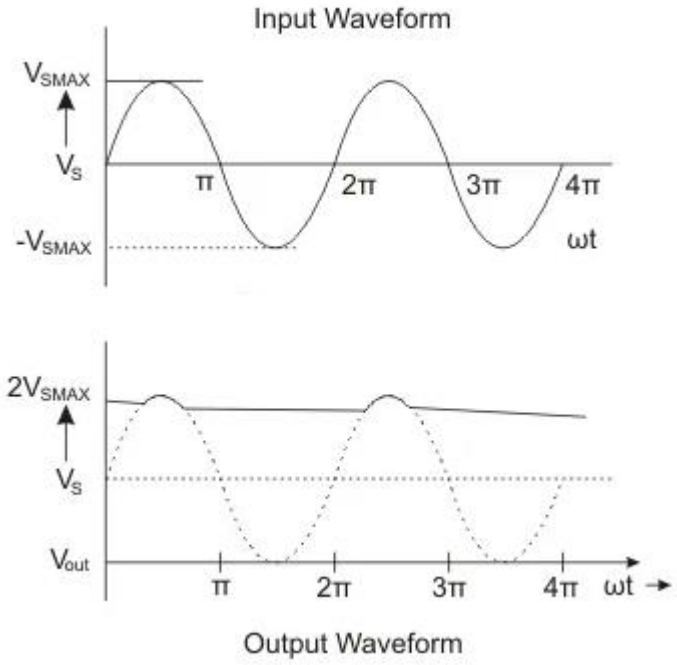
PROCEDURE :

1). Connected the circuit as per the circuit diagram.
2). Switched ON the FG & CRO
3) Applied the $5V_{p-p}$, 1KHz. Sine wave signal from the function generator.
4). Drawn the input and output waveforms from the CRO into the Graph sheet.
5). From the graph calculated the peak to peak voltage and noted down into the tabular form.
6) From the tabular form I noticed that the output DC voltage is approximately doubled to input AC Voltage.
7). I did the same experiment in Multisim software and observed the same thing.

TABULAR FORM :

	Software			**Hardware**	
Sl.No.	**Input AC Voltage In Volts**	**Output DC Voltage In Volts**		**Input AC Voltage In Volts**	**Output DC Voltage In Volts**
1					
2					

EXPECTED WAVEFORMS :



RESULT :

I verified the Voltage doubler Experiment.

VIVA VOCE QUESTIONS:

1. What is voltage doubler ?

2. How do you make a voltage doubler circuit?

3. How does a voltage Quadrupler work?

4. What are the advantages of using voltage doubler?

5. What is half wave voltage doubler ?

6. What is full wave voltage doubler ?

7. What is the difference between the Full wave and Half wave voltage doubler ?

8. What are current multipliers ?

9. How many diodes are there in Half wave voltage doubler ?

10. How many diodes are there in Full wave voltage doubler ?

A. DATA SHEETS

PN JUNCTION DIODE

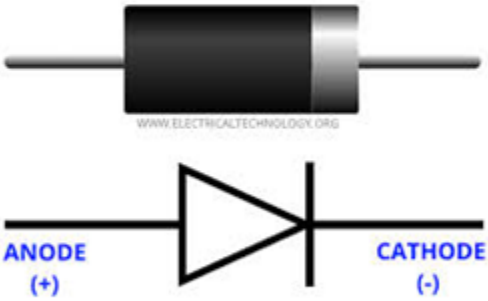
1N4001 - 1N4007 1.0A

Features

- Diffused Junction
- High Current Capability and Low Forward Voltage Drop
- Surge Overload Rating to 30A Peak
- Low Reverse Leakage Current
- **Lead Free Finish, RoHS Compliant (Note 3)**

Mechanical Data

- Case: DO-41
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminals: Finish - Bright Tin. Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band
- Ordering Information: See Page 2
- Marking: Type Number
- Weight: 0.30 grams (Approximate)



Maximum Ratings and Electrical Characteristics (@T_A = +25°C unless otherwise specified.) Single phase, half wave, 60Hz, resistive or inductive load.

For capacitive load, derate current by 20%.

Characteristic	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RW} $_M V_R$	50	100	200	400	600	800	1000	V
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	V
Average Rectified Output Current (Note 1) @ T_A =+75°C	I_O	1.0							A
Non-Repetitive Peak Forward Surge Current 8.3ms Single Half Sine-Wave Superimposed on Rated Load	I_{FSM}	30							A
Forward Voltage @ I_F = 1.0A	V_{FM}	1.0							V
Peak Reverse Current @T_A = +25°C at Rated DC Blocking Voltage @ T_A = +100°C	I_{RM}	5.0 50							µA
Typical Junction Capacitance (Note 2)	C_j	15				8			pF
Typical Thermal Resistance Junction to Ambient	$R_{\theta JA}$	100							K/W
Maximum DC Blocking Voltage Temperature	T_A	+150							°C
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to +150							°C

ZENER DIODE – DATA SHEET :

TOSHIBA 1Z6.2~1Z390,1Z6.8A~1Z30A

TOSHIBA ZENER DIODE SILICON DIFFUSED JUNCTION TYPE

1Z6.2~1Z390,1Z6.8A~1Z30A

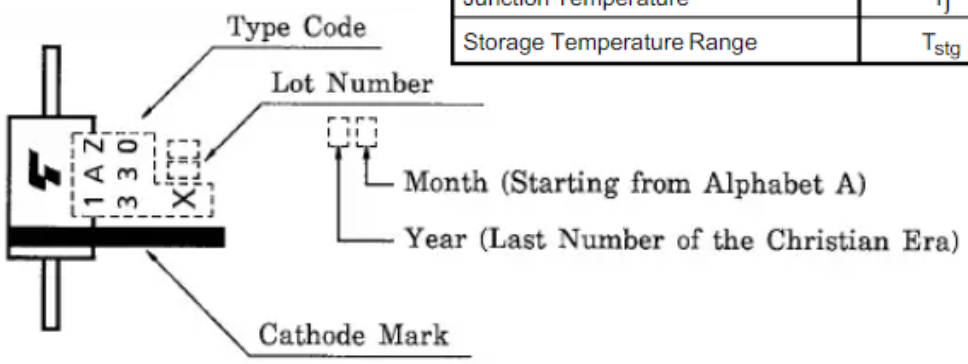
CONSTANT VOLTAGE REGULATION
TRANSIENT SUPPRESSORS

- Average Power Dissipation : P = 1W
- Peak Reverse Power Dissipation : P_{RSM} = 200W at t_W = 200μs
- Zener Voltage : V_Z = 6.2 ~ 390V
- Tolerance of Zener Voltage
  1Z6.2 Series : ±10%
  1Z6.8A Series : ±5%
- Plastic Mold Package

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Dissipation	P	1	W
Junction Temperature	T_j	−40~150	°C
Storage Temperature Range	T_{stg}	−40~150	°C

MARK



Color : Silver

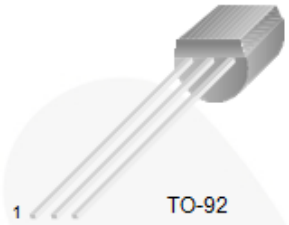
BIPOLAR JUNCTION TRANSISTOR (bjt) – DATA SHEET

FAIRCHILD

BC546 / BC547 / BC548 / BC549 / BC550
NPN Epitaxial Silicon Transistor

Features

- Switching and Amplifier
- High-Voltage: BC546, V_{CEO} = 65 V
- Low-Noise: BC549, BC550
- Complement to BC556, BC557, BC558, BC559, and BC560



TO-92

1. Collector 2. Base 3. Emitter

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{CBO}	Collector-Base Voltage	BC546	80	V
		BC547 / BC550	50	
		BC548 / BC549	30	
V_{CEO}	Collector-Emitter Voltage	BC546	65	V
		BC547 / BC550	45	
		BC548 / BC549	30	
V_{EBO}	Emitter-Base Voltage	BC546 / BC547	6	V
		BC548 / BC549 / BC550	5	
I_C	Collector Current (DC)		100	mA
P_C	Collector Power Dissipation		500	mW
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-Off Current		V_{CB} = 30 V, I_E = 0			15	nA
h_{FE}	DC Current Gain		V_{CE} = 5 V, I_C = 2 mA	110		800	
V_{CE}(sat)	Collector-Emitter Saturation Voltage		I_C = 10 mA, I_B = 0.5 mA		90	250	mV
			I_C = 100 mA, I_B = 5 mA		250	600	
V_{BE}(sat)	Base-Emitter Saturation Voltage		I_C = 10 mA, I_B = 0.5 mA		700		mV
			I_C = 100 mA, I_B = 5 mA		900		
V_{BE}(on)	Base-Emitter On Voltage		V_{CE} = 5 V, I_C = 2 mA	580	660	700	mV
			V_{CE} = 5 V, I_C = 10 mA			720	
f_T	Current Gain Bandwidth Product		V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz		300		MHz
C_{ob}	Output Capacitance		V_{CB} = 10 V, I_E = 0, f = 1 MHz		3.5	6.0	pF
C_{ib}	Input Capacitance		V_{EB} = 0.5 V, I_C = 0, f = 1 MHz		9		pF
NF	Noise Figure	BC546 / BC547 / BC548	V_{CE} = 5 V, I_C = 200 µA, f = 1 kHz, R_G = 2 kΩ		2.0	10.0	dB
		BC549 / BC550			1.2	4.0	
		BC549	V_{CE} = 5 V, I_C = 200 µA, R_G = 2 kΩ, f = 30 to 15000 MHz		1.4	4.0	
		BC550			1.4	3.0	

h_{FE} Classification

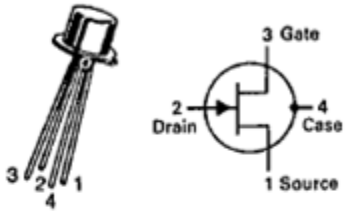
Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800

JUNCTION FIELD EFFECT TRANSISTOR (JFET) – DATA SHEET :

MOTOROLA SC (XSTRS/R F)

BFW10
BFW11

CASE 20-03, STYLE 1
TO-72 (TO-206A)



JFET
VHF/UHF AMPLIFIER

N-CHANNEL — DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Reverse Gate-Source Voltage	V_{GSR}	−30	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.71	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	—	—	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 0.5 nAdc)	BFW10 BFW11	$V_{GS(off)}$	—	—	8 6	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	0.1	nAdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 400 μAdc)	BFW10	V_{GS}	2	—	7.5	Vdc
Gate-Source Voltage (V_{DS} = 15 Vdc, I_D = 50 μAdc)	BFW11	V_{GS}	1.25	—	4	Vdc
ON CHARACTERISTICS						
Zero-Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	BFW10 BFW11	I_{DSS}	8 4	— —	20 10	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz)	BFW10 BFW11	Y_{fs}	3.5 3.0	— —	6.5 6.5	mmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	BFW10 BFW11	Y_{os}	— —	— —	85 50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)		C_{iss}	—	—	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)		C_{rss}	—	—	0.8	pF
Forward Transadmittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 200 MHz)		Y_{fs}	3.2	—	—	mmhos
Equivalent Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 25 Hz)		e_n	—	—	75	$nV/\sqrt{Hz}$
Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0 V, see Figures 1, 2, 3)		NF	—	—	2.5	dB

DATA SHEET OF BF245A; BF245B; BF245C N-CHANNEL SILICON FIELD-EFFECT TRANSISTOR

NXP Semiconductors Product specification

N-channel silicon field-effect transistors

BF245A; BF245B; BF245C

FEATURES

- Interchangeability of drain and source connections
- Frequencies up to 700 MHz.

APPLICATIONS

- LF, HF and DC amplifiers.

DESCRIPTION

General purpose N-channel symmetrical junction field-effect transistors in a plastic TO-92 variant package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	s	source
3	g	gate

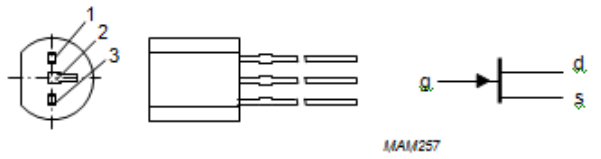


Fig.1 Simplified outline (TO-92 variant) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	±30	V
V_{GSoff}	gate-source cut-off voltage	I_D = 10 nA; V_{DS} = 15 V	–0.25	–	–8	V
V_{GSO}	gate-source voltage	open drain	–	–	–30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF245A		2	–	6.5	mA
	BF245B		6	–	15	mA
	BF245C		12	–	25	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	–	300	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	3	–	6.5	mS
C_{rs}	reverse transfer capacitance	V_{DS} = 20 V; V_{GS} = –1 V; f = 1 MHz; T_{amb} = 25 °C	–	1.1	–	pF

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±30	V
V_{GDO}	gate-drain voltage	open source	–	–30	V
V_{GSO}	gate-source voltage	open drain	–	–30	V
I_D	drain current		–	25	mA
I_G	gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 75 °C;	–	300	mW
		up to T_{amb} = 90 °C; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board, minimum lead length 3 mm, mounting pad for drain lead minimum 10 mm × 10 mm.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	250	K/W
	thermal resistance from junction to ambient		200	K/W

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = –1 μA; V_{DS} = 0	–30	–	V
V_{GSoff}	gate-source cut-off voltage	I_D = 10 nA; V_{DS} = 15 V	–0.25	–8.0	V
V_{GS}	gate-source voltage	I_D = 200 μA; V_{DS} = 15 V			
	BF245A		–0.4	–2.2	V
	BF245B		–1.6	–3.8	V
	BF245C		–3.2	–7.5	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0; note 1			
	BF245A		2	6.5	mA
	BF245B		6	15	mA
	BF245C		12	25	mA
I_{GSS}	gate cut-off current	V_{GS} = –20 V; V_{DS} = 0	–	–5	nA
		V_{GS} = –20 V; V_{DS} = 0; T_j = 125 °C	–	–0.5	μA

Note

1. Measured under pulse conditions: t_p = 300 μs; δ ≤ 0.02.

DYNAMIC CHARACTERISTICS

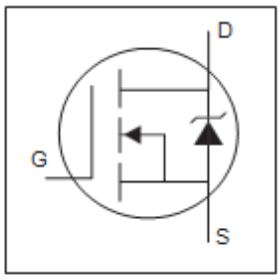
Common source; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 20 V; V_{GS} = −1 V; f = 1 MHz	–	4	–	pF
C_{rs}	reverse transfer capacitance	V_{DS} = 20 V; V_{GS} = −1 V; f = 1 MHz	–	1.1	–	pF
C_{os}	output capacitance	V_{DS} = 20 V; V_{GS} = −1 V; f = 1 MHz	–	1.6	–	pF
g_{is}	input conductance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	250	–	µS
g_{os}	output conductance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	40	–	µS
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	3	–	6.5	mS
		V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	6	–	mS
$\lvert y_{rs} \rvert$	reverse transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	1.4	–	mS
$\lvert y_{os} \rvert$	output admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	–	25	–	µS
f_{gfs}	cut-off frequency	V_{DS} = 15 V; V_{GS} = 0; g_{fs} = 0.7 of its value at 1 kHz	–	700	–	MHz
F	noise figure	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz; R_G = 1 kΩ (common source); input tuned to minimum noise	–	1.5	–	dB

DATA SHEET OF MOSFET IRFZ 44N

IRFZ44NPbF

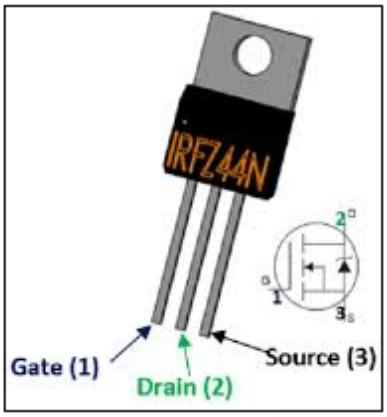
HEXFET® Power MOSFET



V_{DSS} = 55V

$R_{DS(on)}$ = 17.5mΩ

I_D = 49A



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	49	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	35	
I_{DM}	Pulsed Drain Current ①	160	
P_D @T_C = 25°C	Power Dissipation	94	W
	Linear Derating Factor	0.63	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	25	A
E_{AR}	Repetitive Avalanche Energy①	9.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.058	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	17.5	mΩ	V_{GS} = 10V, I_D = 25A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	19	—	—	S	V_{DS} = 25V, I_D = 25A④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	63	nC	I_D = 25A
Q_{gs}	Gate-to-Source Charge	—	—	14		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	23		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 28V
t_r	Rise Time	—	60	—		I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		R_G = 12Ω
t_f	Fall Time	—	45	—		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1470	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	360	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	88	—		f = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	—	530⑤	150⑥	mJ	I_{AS} = 25A, L = 0.47mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	49	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	63	95	ns	T_J = 25°C, I_F = 25A
Q_{rr}	Reverse Recovery Charge	—	170	260	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.48mH R_G = 25Ω, I_{AS} = 25A. (See Figure 12)

③ I_{SD} ≤ 25A, di/dt ≤ 230A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C .

DATA SHEET OF UJT

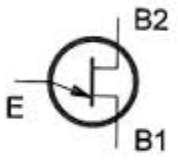
2N2646
2N2647

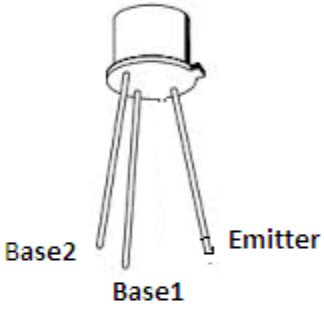
SILICON
PN UNIJUNCTION TRANSISTORS

Central Semiconductor Corp.
www.centralsemi.com

DESCRIPTION:
The CENTRAL SEMICONDUCTOR 2N2646 and 2N2647 devices are silicon PN Unijunction Transistors designed for general purpose industrial applications.

UJT Symbol & Terminal Identification





(a). Symbol **(b). Terminal Identification**

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Emitter Reverse Voltage	V_{B2E}	30	V
Interbase Voltage	V_{B2B1}	35	V
RMS Emitter Current	I_e	50	mA
Peak Emitter Current (Duty Cycle ≤1%, PRR≤10pps)	i_e	2.0	A
RMS Power Dissipation	P_D	300	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

		2N2646		2N2647		
SYMBOL	**TEST CONDITIONS**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
η	V_{B2B1}=10V	0.56	0.75	0.68	0.82	
R_{BB}	V_{B2B1}=3.0V	4.7	9.1	4.7	9.1	kΩ
I_{EB2O}	V_{B2E}=30V	-	12	-	0.2	μA
I_V	V_{B2B1}=20V, R_{B2}=100Ω	4.0	-	8.0	18	mA
I_P	V_{B2B1}=25V	-	5.0	-	2.0	μA
V_{OB1}	V_1=20V	3.0	-	6.0	-	V

B. RULES TO BE FOLLOWED WHILE OPERATING THE REGULATED POWERSUPPLY(RPS)

The flowing rules should be followed before switch ON the Regulated Power Supply,

1. Initially Keep the *voltage Course & Voltage fine controls* of RPS at minimum position. Later (After switch ON the RPS) can vary these controls slowly to get the required voltage.
2. Always keep the Current Limit control at maximum position, Otherwise the display can shows the constant voltage instead of varying.

Trouble shooting while operating the *rps* :

The following trouble shooting can done while operating the RPS,

During connecting the RPS to the circuit and varying the Voltage Course & Voltage Fine Controls, If it displays the voltage as constant or above 30V then it can said that either the circuit is shorted OR the Current Limit control is not kept at maximum position. This problem can solve to prevent the circuit from shorted and by keeping the Current Limit control at maximum.

RULES TO OPERATE THE CRO:

The following rules should be follows before operate the CRO.

1. Keep the following controls at middle position or vary until the electron beam is generated.
   a) INTENSITY b) FOCUS c) ⇔ (Horizontal position)
   (Horizontal position common for both channels)
   d) ⇕ Vertical Position (Vertical position individual per each channel) e) LEVEL (Trigger Level)
1. Keep the following controls at maximum position.
   (a). VARIABLE controls of VOLTS/DIV switch in both channels.
   (b). SWP.VAR (Sweep Variation)
2. Keep the following switches at releasing mode.
   a) ×10 MAG b) TRIG.ALT c) SLOPE d) ALT/CHOPe) CH2 INV
3. Initially should keep the **TIME/DIV** control at 1mS position, later can change this switch depending upon our requirement , i.e. if we can't get the signal clearly on the CRT, then we can vary this switch until to get the signal.
4. Set the channel selector control **MODE** at the appropriate position i.e. if we want to seethe signal in channel1, set this control at CH1, in channel2 set at CH2, in both channels set at DUAL. To add the signals (algebraically sum or difference) available in both channels set atADD.
5. **AC/GND/DC**: Before setting the signals on CRT, first we should keep the electron beam on referenceline. To set this beam on reference line, keep this control at GND positio and then vary vertical position control until to get the beam on the reference line. After that to see the applied signals, keep this control at AC or DC positions.
6. Always keep the **TRIGGER MODE** control at AUTO position.
7. Keep the **SOURCE** control at approximate channel. It means if MODE control is selectedto CH1, then the SORCE control should select to CH1. If MODE control at CH2, set the SOURCE control at CH2. If MODE control at DUAL or ADD, set the SOURCE control either at CH1 or CH2.

C. Rules for how to write the observation and records:

1. Make the top & right margins in each page of right side.
2. In top margin make the headings as Experiment No., date and name of the experiment.
3. Circuit diagrams, tabular columns, expected graphs and parameters/calculations should write on leftside page (even No. page) .
4. Aim, apparatus, components, theory, procedure, applications, conclusion and result should write onright side page (Odd No. Page) .
5. Headings should underline with any other ink except red, orange and green.
6. The every new experiment should start with right side page.
7. leave the half of the page under the heading of *theory*.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

B.Tech –II-I Sem 19A04302P ELECTRONIC DEVICES AND CIRCUITS LAB

LIST OF EXPERIMENTS: **Branch : For ECE only** **R19**

12. Verification of Volt-Ampere characteristics of a PN junction diode and find static, dynamic and reverse resistances of the diode from the graphs obtained.

13. Design a full wave rectifier for the given specifications with and without filters, and verify the given specifications experimentally. Vary the load and find ripple factor. Draw suitable graphs.

14. Verify various clipping and clamper circuits using PN junction diode and draw the suitable graphs.

15. Design a Zener diode based voltage regulator against variations of supply and load. Verify the same from the experiment.

16. Study and draw the output and transfer characteristics of MOSFET (Enhance mode) in Common Source Configuration experimentally. Find Threshold voltage (v_T), g_m, & K from the graphs.

17. Study and draw the output and transfer characteristics of MOSFET (Depletion mode) or JFET in Common Source Configuration experimentally. Find I_{DSS}, gm, & V_P from the graphs.

18. Verification of the input and output characteristics of BJT in Common Emitter configuration experimentally and find required h –parameters from the graphs.

19. Study and draw the input and output characteristics of BJT in Common Base configuration experimentally, and determine required h –parameters from the graphs.

20. Verify the Volt Ampere characteristics of SCR experimentally and determine holding current and break over voltage from the graph.

21. Study and draw the Volt Ampere characteristics of UJT and determine η, I_P, Iv, V_P , & Vv from the experiment.

22. Design and analysis of voltage-divider bias/self bias circuit using BJT.

12. Design and analysis of voltage-divider bias/self bias circuit using JFET.

13. Design and analysis of self bias circuit using MOSFET.

14. Design a suitable circuit for switch using CMOSFET/JFET/BJT.

Note: All the experiments shall be implemented using both Hardware and Software. Student has to perform minimum of any 12 experiments.