



# SVR ENGINEERING COLLEGE

Service Virtue Reverence

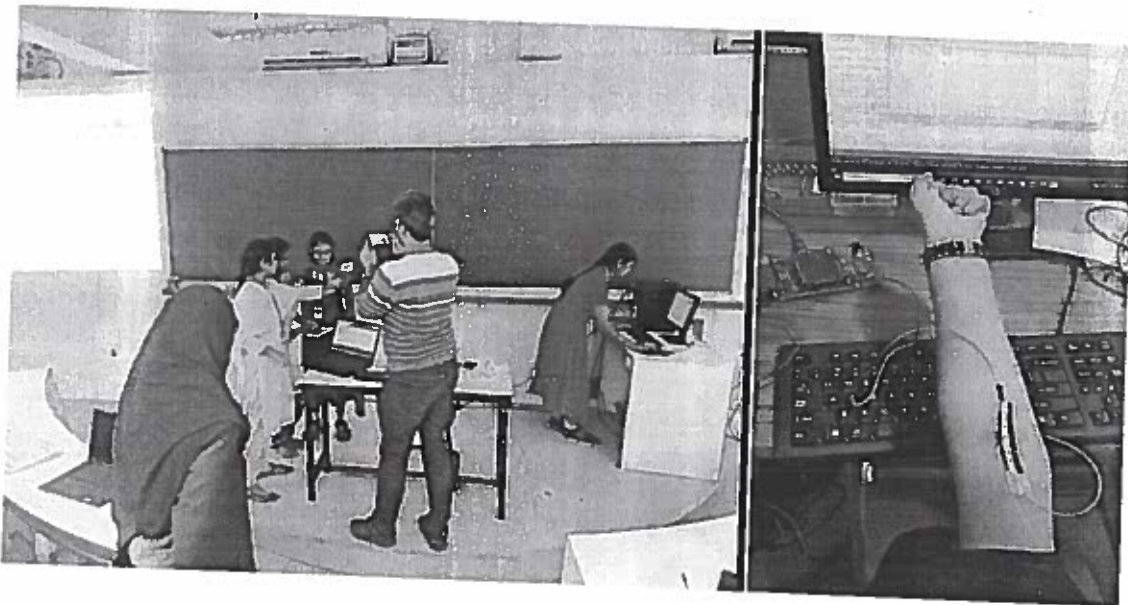
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SVR Engineering College has initiated an innovation ecosystem to inculcate research activities among students and faculty members.

## A NOVEL LOW COST WEARABLE SENSOR USING VELOSTAT:

The Speech recognition technology is continuously improving which is making way for innovative ideas to come up. This technology is widely used and implemented across various platforms. The communication between the human speech and the computer application which recognize the speech is only possible by interfacing.

Velostat is a low-cost, low-profile electrical bagging material with piezoresistive properties, making it an attractive option for in-socket pressure sensing. The focus of this research was to explore the suitability of a Velostatbased system for providing real-time socket pressure profiles. The prototype system performance was explored through a series of bench tests to determine properties including accuracy, repeatability and hysteresis responses, and through participant testing with a single subject.



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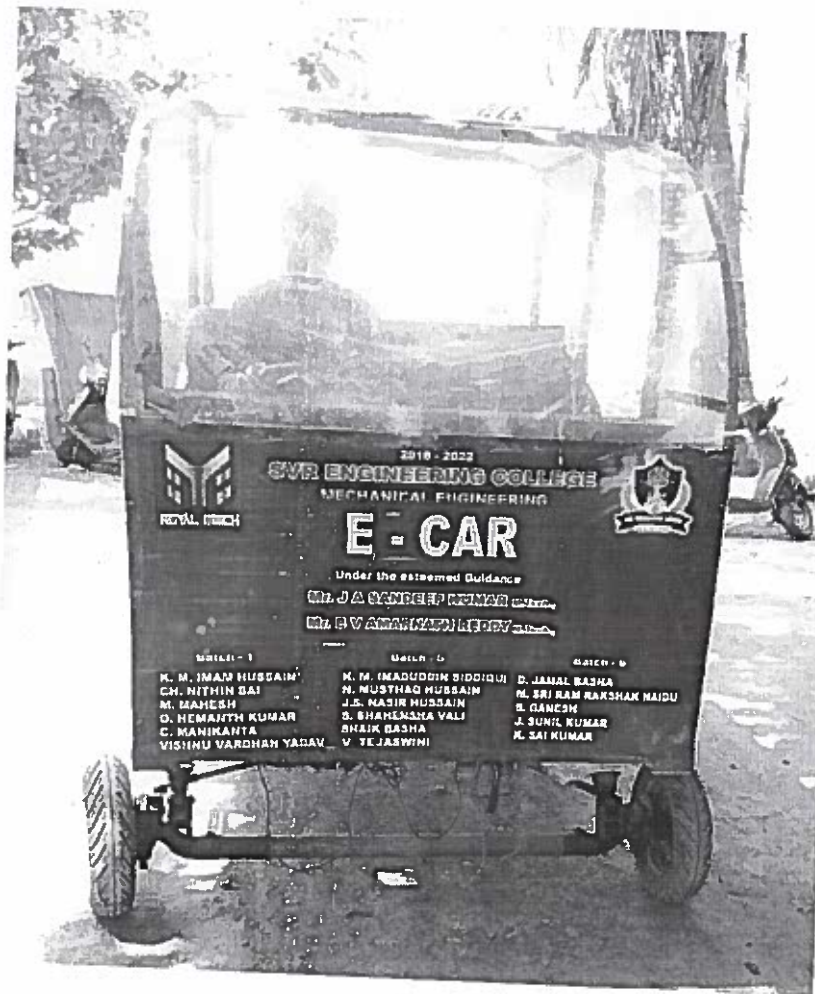
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## Battery Electric Vehicle: An Emerging Technology:

As concerns of oil depletion and security of supply remain as severe as ever, and faced with the consequences of climate change due to greenhouse gas emissions, India and other European countries increasingly looking at alternatives to traditional road transport technology. Battery electric vehicle as seen as promising technology, which could lead to the decarbonisation of the light duty vehicle fleet and to independence from oil.



  
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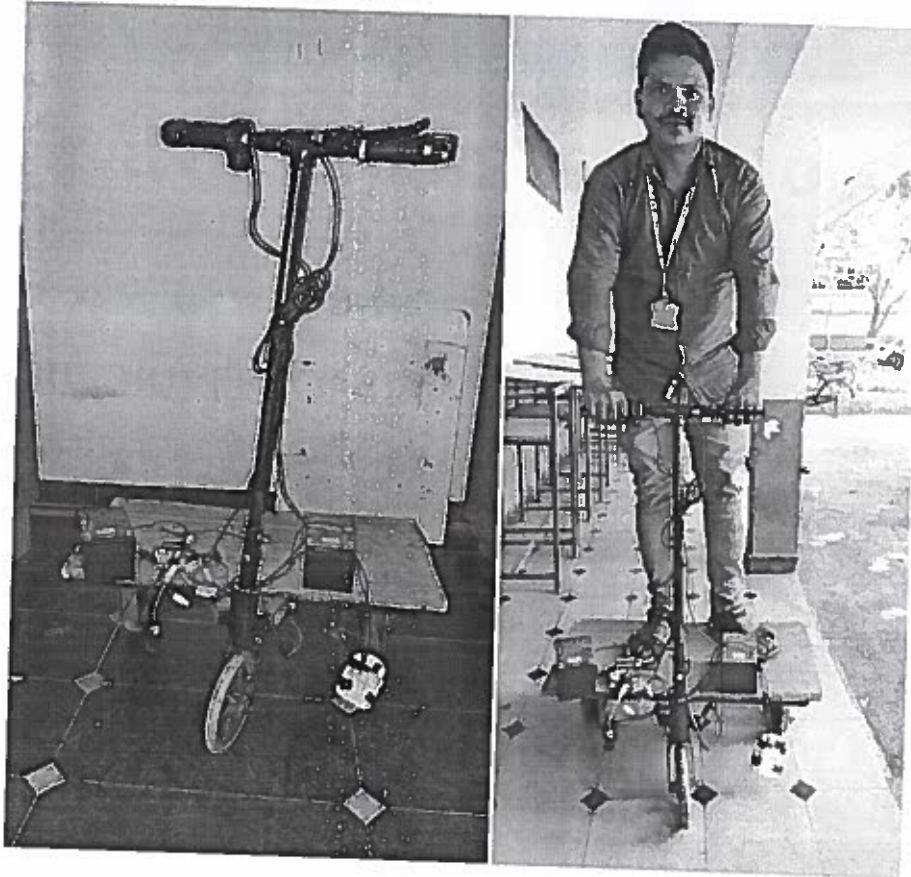
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## ELECTRIC HOVERBOARD:

A hoverboard has two large wheels separated by a long board and it is powered by electricity through battery. The hover board allows riders to move across the ground without pedalling or pushing with their feet.



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(12) PATENT APPLICATION PUBLICATION

(19) INDIA

(22) Date of filing of Application :20/09/2022

(21) Application No.202211053618 A

(43) Publication Date : 07/10/2022


(54) Title of the invention : SYSTEMATIC FRAMEWORK FOR SMARTER CONSTRUCTION TECHNIQUES THROUGH ACCOMPLISHING GREEN BUILDING INITIATIVE WITH ZERO WASTE MANAGEMENT

(51) International classification : A61F0013150000, B01D0061020000, G06Q0050080000, C02F0001440000, E04C0002040000  
(86) International Application No : NA  
Filing Date : NA  
(87) International Publication No : NA  
(61) Patent of Addition to Application Number : NA  
Filing Date : NA  
(62) Divisional to Application Number : NA  
Filing Date : NA

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(57) Abstract :  
Systematic framework for Smarter Construction techniques through accomplishing Green Building initiative with Zero Waste Management is the proposed invention. The proposed invention implements a framework of systematic approach to integrate the green building techniques in construction. The invention aims at achieving zero waste management by improving the tasks of recycling and correct disposal. The intention is to reduce waste and initiate green building.

No. of Pages : 13 No. of Claims : 7

  
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(12) PATENT APPLICATION PUBLICATION

(19) INDIA

(22) Date of filing of Application : 25/09/2018

(21) Application No 201841036063 A

(43) Publication Date : 05/10/2018

(54) Title of the invention : A DEVICE FOR DETECTING SYNTHETIC FOOD INGREDIENTS


(51) International classification : A61K35/00;  
A61K36/00  
(31) Priority Document No : NA  
(32) Priority Date : NA  
(33) Name of priority country : NA  
(86) International Application No : NA  
Filing Date : NA  
(87) International Publication No : NA  
(61) Patent of Addition to Application Number : NA  
Filing Date : NA  
(62) Divisional to Application Number : NA  
Filing Date : NA

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5) Dr. S. CHIDAMBARANATHAN  
6) MD. RAFEEQ  
7) BETALA RAKESH  
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9) KORRA SEENA NAIK  
10) K. S. R. K. SARMA  
11) Dr. SUDARSHAN. E  
12) DR. CHANDRASHEKHAR. A  
13) SHANKARNAYAK BHUKYA

(57) Abstract :

Present invention relates to a device for detecting synthetic food products. More particularly, the invention relates to a device for detecting synthetic rice and egg. Moreover, the device is designed to automatically connect to a smart electronic device for cooking rice and egg. The device comprises of a pressure applying chamber for detecting of synthetic grains and furthermore, an imaging plate to recognize the synthetic eggs kind of food ingredients.

No. of Pages : 16 No. of Claims : 8

  
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(12) PATENT APPLICATION PUBLICATION

(19) INDIA

(22) Date of filing of Application : 23/12/2019

(21) Application No. 201941053591 A

(43) Publication Date : 18/09/2020

(54) Title of the invention : AN EFFICIENT ARITHMETIC VLSI ARCHITECTURE FOR DWPT ERROR APPROXIMATION

(51) International classification

:H03H0017060000,  
H03H0017020000,  
G06F0007544000,  
G06F0007523000,  
G06F0017500000

(31) Priority Document No

:NA

(32) Priority Date

:NA

(33) Name of priority country

:NA

(86) International Application No

:NA

Filing Date

:NA

(87) International Publication No

:NA

(61) Patent of Addition to Application Number

:NA

Filing Date

:NA

(62) Divisional to Application Number

:NA

Filing Date

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8) JYOTHI. CHINNA BABU

9) Prof. D SURENDRA RAO

10) Prof. V. BHAGYA RAJU

11) S. Hemanth chowdary

12) Ravinder Korani

13) MAHESH ENUMULA

14) T SYED AKHEEL

15) Mude Sreenivasulu

(57) Abstract :

The power budget, size and cost make the task difficult to integrate more functions as the signal processing algorithms such as Discrete wavelet transform (DWT), Discrete wavelet packet transform (DWPT), finite impulse response (FIR) filtering. Therefore, developing low-complexity hardware efficient arithmetic design for healthcare application remains a challenge. DSP algorithms are implemented in dedicated hardware system to meet space-time requirement of resource constrained applications such as repetitive multiply-accumulate operations, computational symmetry and redundancy. Efficient implementation of multiplication operations is a key issue in digital filter design of DSP application. Separate approach is used for signed and unsigned multiplication. Approximate multiplication and addition operation provide small area and leakage power due to saving of storage data-bits. Approximate computation methodology produces dynamic power reduction due to memory access saving. Approximate computation consider small percentage of accuracy loss that does not affect much the overall application specific performance in digital arithmetic hardware design. Delay and power consumption is considered to be major issue in ripple carry adder (RCA) design is required to study the effectiveness of the arithmetic coefficient approximation method on DWPT computation. The bit level optimization of full-width adder tree for multiple constant multiplication (MCM) is given to taking the advantage of shifting operation. Considered images with different colour and edge information for DWPT applications are grouped as low-texture, moderate-texture and higher-texture images for discussion purpose. Less colour variation with less edge information refer to low-texture image, less colour variation with more edge information refer to moderate-texture image, and more colour variation with more edge information refer to higher-texture image. Pixel variation is more in data-vectors of higher-texture images, relatively less in data-vectors of moderate-texture images and almost absent/small in data-vectors of low-texture images. The proposed shift-add register (SAR) and approximate arithmetic architecture designs use a fixed-bias for error-compensation. The fixed-bias compensates truncation error near accurately for input data-vector with more pixel variation while overcompensate the truncation error for input data-vector with small pixel variation.

No. of Pages : 15 No. of Claims : 2

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41014

The Patent Office Journal No. 38/2020 Dated 18/09/2020

PATENT APPLICATION PUBLICATION

(19) INTRA

(22) Date of filing of Application: 09/08/2020

(21) Application No. 20204101317A

(43) Publication Date: 04/09/2020

(54) Title of the Invention: CREDIT CARD FRAUD DETECTION INTELLIGENT PROCESS TO CREDIT CARD FRAUD DETECTION USING DEEP LEARNING, MACHINE LEARNING

(51) International classification : G06Q20/4016  
 (31) Priority Document No : NA  
 (32) Priority Date : NA  
 (33) Name of priority country : NA  
 (85) International Application No : NA  
 Filing Date : NA  
 (87) International Publication No : NA  
 (61) Patent of Addition to Application Number : NA  
 Filing Date : NA  
 (62) Divisional to Application Number : NA  
 Filing Date : NA

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(57) Abstract :  
 ABSTRACT My invention Credit Card Fraud Detection is a intelligent system and process to detects fraudulent transactions using a intelligent predictive model such as a deep learning programming, neural network to evaluate individual customer accounts (through Credit Card) and identify potentially fraudulent transactions (time maximum 24 H) based on learned relationships, global bank data server among known variables. The invented system may also output reason codes indicating relative contributions of various variables to a particular result and the system periodically (per transaction track the register mobile location and credit card location accordingly detect) monitors its performance and redevelops the model when performance drops below a predetermined level. The invention also give the probability may then be provided as output to a human decision-maker involved in processing the per transaction with both location matching (credit card, mobile no) or the issuer may be signaled when the probability exceeds a predetermined amount. The effective fraud detection model generally requires more variables than conventional parameter analysis systems can handle and also in order to capture new fraud schemes, parameter analysis systems must be redeveloped often, and automated redevelopment is difficult to implement.

No. of Pages : 28 No. of Claims : 10

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(12) PATENT APPLICATION PUBLICATION  
(19) INDIA

(21) Application No.202141008336 A

(22) Date of filing of Application :27/02/2021

(43) Publication Date : 05/03/2021

(54) Title of the invention : SELF HEALING COMPOSITE

(51) International classification	:C04B0111340000, C04B0020100000, C04B0028020000, C04B0111720000, C04B0014020000	(71)Name of Applicant : 1)Dr.T.Chandra Sekhara Reddy Address of Applicant :Professor of Civil, Engineering Department, G Pulla Reddy Engineering College, Kurnool- 518007, Andhra Pradesh, India. Andhra Pradesh India 2)Mr.A.Raviteja 3)Dr.C.Sashidhar
(31) Priority Document No	:NA	(72)Name of Inventor : 1)Dr.T.Chandra Sekhara Reddy 2)Mr.A.Raviteja 3)Dr.C.Sashidhar
(32) Priority Date	:NA	
(33) Name of priority country	:NA	
(86) International Application No	:NA	
Filing Date	:NA	
(87) International Publication No	:NA	
(61) Patent of Addition to Application Number	:NA	
Filing Date	:NA	
(62) Divisional to Application Number	:NA	
Filing Date	:NA	

(57) Abstract :

ABSTRACT: Title: Self Healing Composite A self-repairing concrete includes crystalline admixture and silica fume, in which the crystalline admixture and silica fume are mixed for a fixed function of micro-cracks. The quality mixture ratio is: concrete/water=100:1-15:15-50. The manufacturing method is weighing a full amount of water in a container, adding crystalline admixture and silica fume, stirring; pouring the water into the mixing container, adding the corresponding quality of cement; stirring; adding sand and gravel filling materials, conducting worksite watering, volume for each time, vibrating, and air exhausting; until the paste filling mold.

No. of Pages : 17 No. of Claims : 10

  
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